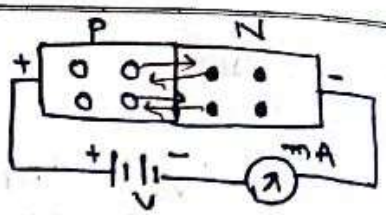
OPAMP

CP-1 P-N Junction Diode



Working of Diode :-

Forward bias :-

* when an external voltage is applied to P-N junction in such a direction that it cancels the potential barrier and permits the current flow is called as forward bias.
* To apply a forward bias, the +ve terminal of a battery is connected to P-type semiconductor while the negative terminal is connected to N-type semiconductor.
* The applied forward potential establishes an electric field opposite to the potential barrier.
* The potential barrier is very small (0.3 volt for Ge and 0.7 volt for Si), therefore, a small forward voltage is sufficient to completely eliminate the potential barrier.
* when potential barrier is eliminated by the forward voltage, junction resistance becomes almost zero & current flows across P-N junction Diode.
* In case of the forward bias, the holes from P-type semiconductor are repelled by the +ve battery terminal towards the junction & the electrons in N-type semiconductor are repelled by -ve battery terminal towards junction.
* Here, the battery voltage should be high into to move the charge carrier across the potential barrier.
* when an electron hole combination takes place near the junction, a covalent bond near the

Covalent bond -: Sharing of electron pair betn atoms.

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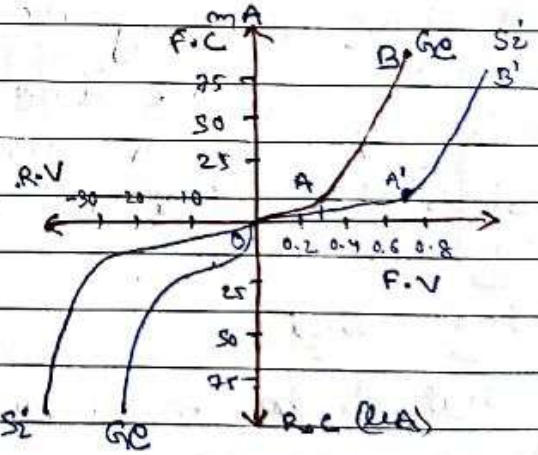
Positive terminal of a battery breaks down & electron will enter to the +ve terminal. (P-region)

* Due to the combination, a free space will be created near the junction.
* The constant movement of electrons towards the positive terminals and the holes towards the -ve terminal produces a high forward current.

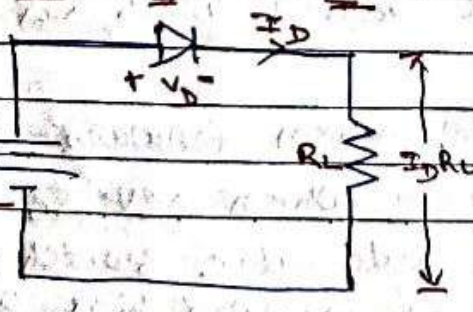
Reversed biased -:

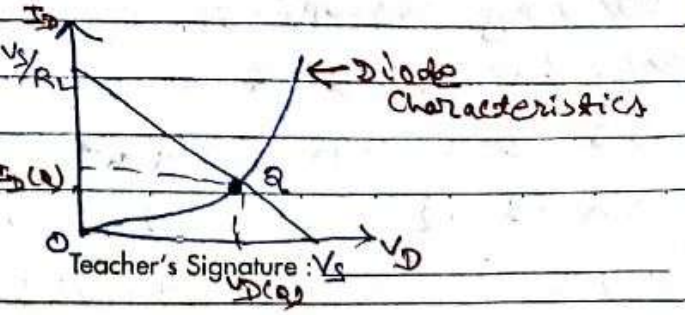
* when an external voltage is applied to P-N junction in such a direction that it increases the potential barrier, it is called as reverse bias.
* For reversed bias, the positive terminal of the battery is connected to N-type semiconductor and -ve terminal is connected to P-type semiconductor.
* Here both the charge carriers attracted toward the respective terminal, so that potential barrier will be wider & current is not flowing during this condition.

V-I Characteristics of Diode



D.C. LOAD LINE -:





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*Consider a diode connected in series with a load resistance R_L across a supply voltage V_S.

* Here, the diode is forward biased.

* A line drawn on the characteristics of the device that represents all d.c. conditions that could exist within the circuit for given values of V_S & R_L is called as d.c. load line.

* By applying KVL

$$V_S - V_D - I_D R_L = 0$$

$$\Rightarrow I_D = \frac{V_S}{R_L} - \frac{V_D}{R_L}$$

Case-(1) when $V_D = 0$

$$\Rightarrow \boxed{I_D = \frac{V_S}{R_L}}$$

Case-(2) when $I_D = 0$

$$\boxed{V_D = V_S}$$

* A line passing through the points (V_S/R_L) and V_S is called a load line.

* The intersection point bet^n D.C load line & diode characteristics line is called as bias point & is denoted by 'Q'.

Important terms:-

a) Ideal diode:-

→ An ideal diode is a two terminal device which has the following properties.

a) conducts with zero resistance when forward-biased &

b) offers an infinite resistance when reverse-biased.

→ An ideal diode acts like an automatic switch. The switch is closed when the diode is forward bias and

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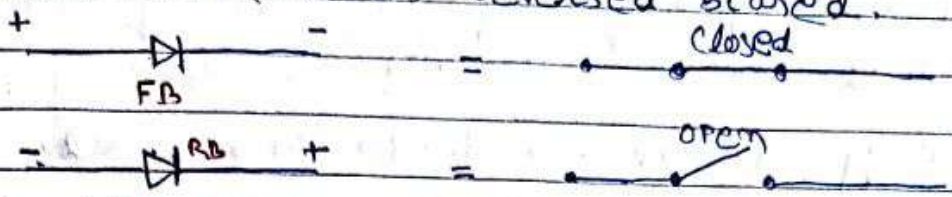
is open when it is reversed biased.



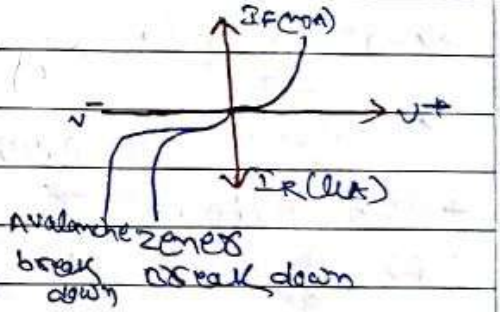
Knee voltage :-

→ Knee voltage is defined as the forward voltage at which the current through the junction starts increasing rapidly.

→ when a diode is FB, the forward current increases very slowly in the beginning. After it exceeds the knee voltage, the current starts increasing rapidly.

* Knee voltage of Si = 0.7 volt, Ge = 0.3 volt.

Zener breakdown



→ The zener breakdown takes place in junctions which are heavily doped (having narrow depletion layers).

→ when breakdown voltage is applied, a very strong electric field appears across the narrow depletion layer which breaks the bonds & electron-hole pairs are generated.

→ A small further increase in reverse voltage produces large no. of current carriers which suddenly increase the reverse current.

Avalanche breakdown :-

→ The avalanche breakdown occurs in junctions which are lightly doped (having wide depletion layers) and the electric field across the junction is not so strong to produce zener breakdown.

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P-N Diode Clipping Circuits :- Used :- to protect the electronic devices from over voltage condⁿ

* A wave shaping circuit which controls the shape of output waveform by removing or clipping a portion of the applied wave is known as clipping circuit.

* For a clipping circuit, a diode (which acts as a closed switch when forward-biased & an open switch when reversed biased) & a resistor are required.

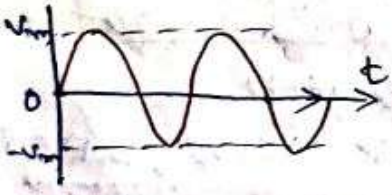
* Here we used AC voltage source for clipping purpose, but sometimes we used a DC battery for this purpose.

* It is of 3 types.

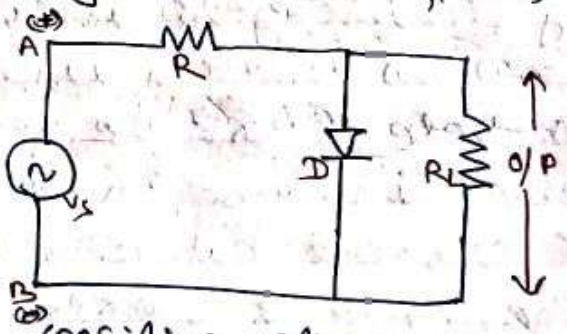
a) positive & negative clippers :-

→ positive clipper :-

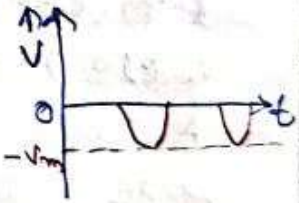
* The clipper which removes the positive half-cycles of the input voltage is known as positive clipper.



(Input wave form)



(positive clipper)



(Output waveform)

During the +ve half cycle,

* when 'A' is +ve w.r.t 'B', the diode (D) is Forward-biased & it acts like a closed switch. (short ckt)

* Here voltage drop across the diode or across the load resistor R_L is zero. So the output during the +ve half cycle will be zero.

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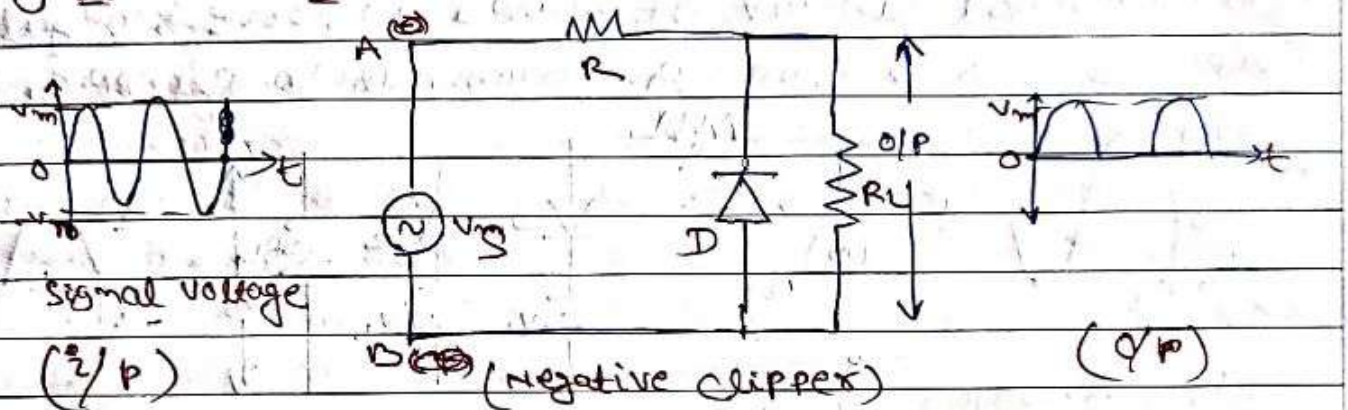
* During the -ve half cycle, when 'B' is +ve w.r.t 'A', the diode (D) is Reversed-biased & it acts like a open switch.
* Here the entire i/p voltage appears across the load resistor (R_L)

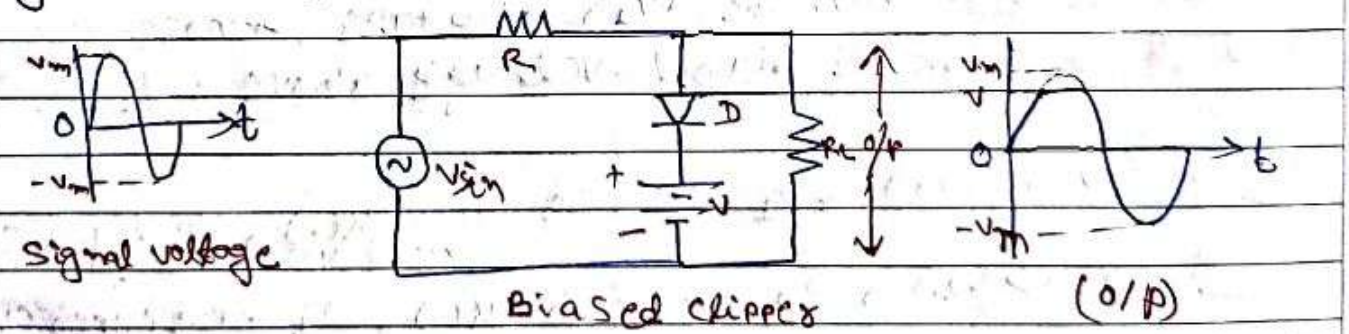
output voltage $= \frac{R_L}{R+R_L} V_m$

Negative clipper :-



Biased clipper :-

→ A biased clipper is used, when it is desired to remove a small portion of positive or negative cycle of the signal voltage.



case (1) :- $V_{in} < V$ for +ve half cycle :-

* In this case, the diode (D) is reverse-biased & it acts as an open ckt. Therefore, most of the i/p voltage appears across the o/p.

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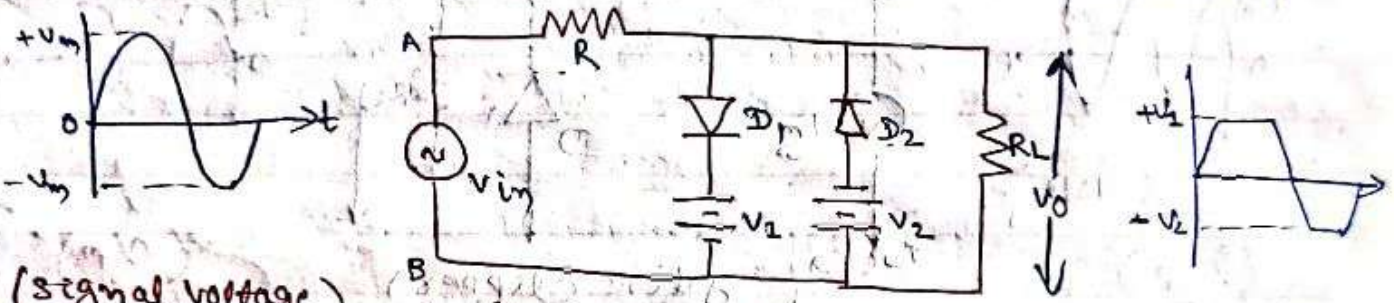
Case ② -: $V_{in} > V$ for positive half cycle -:
→ In this case, the Diode (D) is forward biased.
→ The O/P voltage is equal to $+V$.
Case ③ -: Vin is negative -:
→ In this case, the diode D is reverse-biased & acts as open switch.
→ Therefore, entire -ve half cycle appears across the load.

Combination clipper

* A combined circuit of biased positive & negative clippers is known as combination clipper.



(signal voltage) Combination clipper ckt) (O/P waveform)

Case-1 ($V_{in} < V_1$) D_1, D_2 = RB (open ckt.), O/P Vtg. = $+V_1$

Case-2 when +ve I/P voltage (V_{in}) > $+V_1$, diode (D_2) is forward-biased while diode D_2 is reversed-biased.
→ Therefore, a voltage ($+V_1$) appears across the load and the positive signal voltage above $+V_1$ is clipped off.

Case-3 ($V_{in} < V_2$), D_1, D_2 = RB (open ckt.), O/P Vtg = $-V_2$

Case-4 ($V_{in} > V_2$), D_2 = FB (Sh. ckt.), D_1 = RB (open ckt.)
→ Therefore, a voltage ($-V_2$) appears across the load & the negative signal voltage above $-V_2$ is clipped off.

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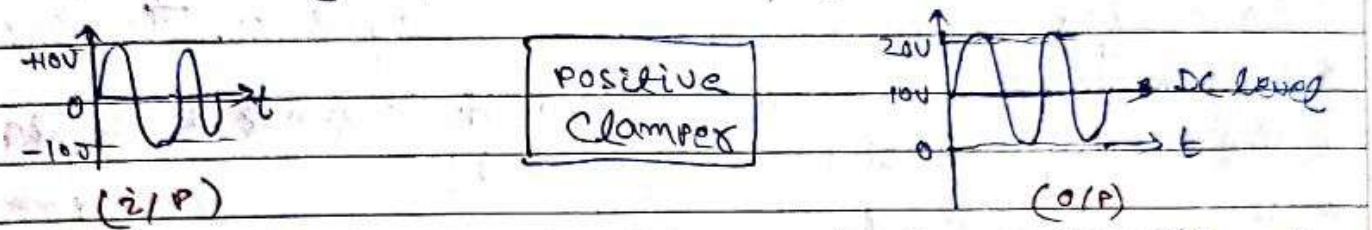
P-N Diode clamping ckts :-

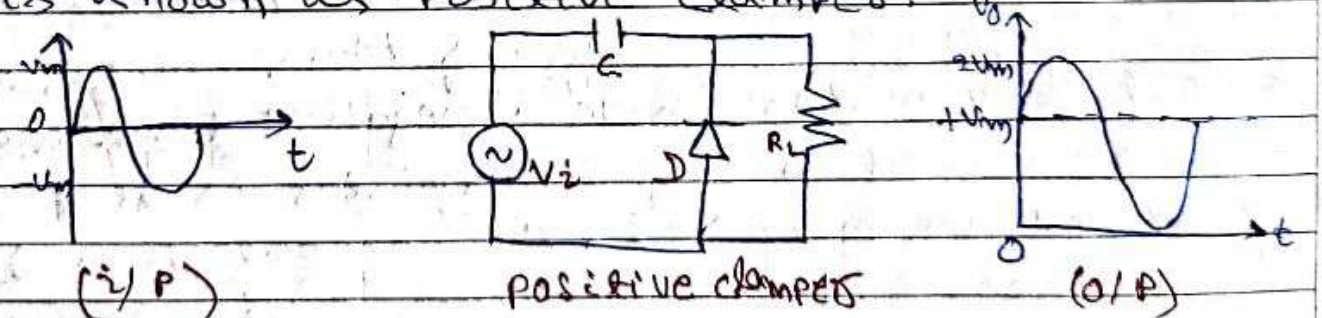
* Clamping is a process of introducing a d.c level into an ac signal. (Restore dc value in AC waveform) (without changing the shape of applied signal)
* A clamping circuit is a device that places either the positive or negative peak of a signal at a desired level.



* For clamping ckt, we required a diode, a capacitor & a resistor.
* Here, the waveforms of i/p & o/p remain the same, of course, there is a vertical shift either upward or downward.

positive clamper :-

* when a clamper shifts the original signal in vertical upward direction in such a way that the negative peak of the signal falls on zero level, it is known as positive clamper.



Negative clamper :-

* when a clamper shifts the original signal in vertical downward direction in such a way that the positive peak of the signal falls on zero level, it is known as negative clamper.

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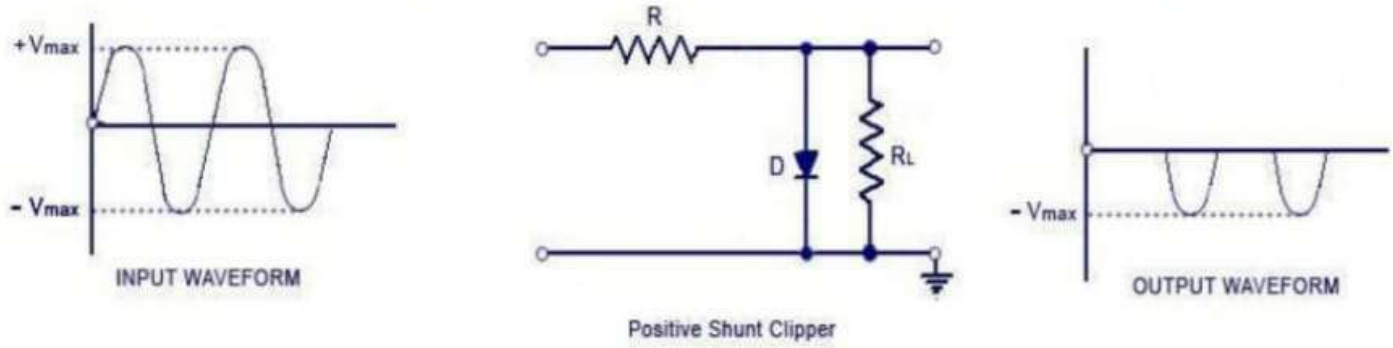
➢ CLIPPING CIRCUITS

- The circuit with which the waveform is shaped by removing (or clipping) a portion of the applied wave is known as a clipping circuit.
- Clippers find extensive use in radar, digital and other electronic systems.
- Although several clipping circuits have been developed to change the wave shape, we concentrate only on diode clippers.
- These clippers can remove signal voltages above or below a specified level.
- The important diode clippers are:-
    1. Positive clipper and negative clipper
    2. Biased positive clipper and biased negative clipper
    3. Combination clipper.

➢ POSITIVE CLIPPER

- A positive clipper is that which removes the positive half-cycles of the input voltage.
- The positive clipper is of two types
    1. Positive series clipper
    2. Positive shunt clipper
- The below Fig. shows the typical circuit of a positive shunt clipper using a diode.



- Here the diode is kept in parallel with the load.
- During the positive half cycle, the diode 'D' is forward biased and the diode acts as a closed switch. This causes the diode to conduct heavily.
- This causes the voltage drop across the diode or across the load resistance R_L to be zero. Thus output voltage during the positive half cycles is zero.
- During the negative half cycles of the input signal voltage, the diode D is reverse biased and behaves as an open switch. Consequently the entire input voltage appears across the diode or across the load resistance R_L if R is much smaller than R_L
- Actually the circuit behaves as a voltage divider with an output voltage of $-[R_L / R+ R_L]$ $V_{max} \cong -V_{max}$ (Taking or assuming when $R_L >> R$).

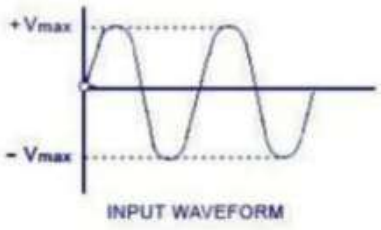
➢ NEGATIVE CLIPPER

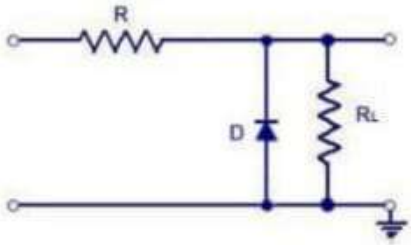
➢ A negative clipper is that which removes the positive half-cycles of the input voltage.

The negative clipper is of two types

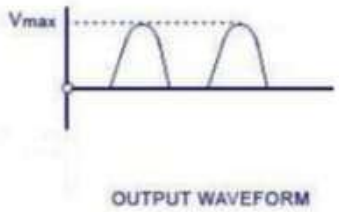
1. Negative series clipper
2. Negative shunt clipper

➢ The below Fig. shows the typical circuit of a negative shunt clipper using a diode.





Negative Shunt Clipper



➢ During the negative half cycle, the diode 'D' is forward biased and the diode acts as a closed switch. This causes the diode to conduct heavily.

➢ This causes the voltage drop across the diode or across the load resistance R_L to be zero. Thus output voltage during the negative half cycles is zero.

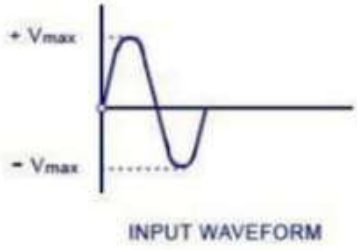
➢ During the positive half cycles of the input signal voltage, the diode D is reverse biased and behaves as an open switch. Consequently the entire input voltage appears across the diode or across the load resistance R_L if R is much smaller than R_L

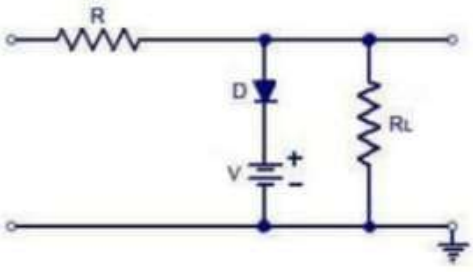
➢ Actually the circuit behaves as a voltage divider with an output voltage of $[R_L / R+ R_L]$ $V_{max} \cong V_{max}$ (Taking or assuming when $R_L >> R$).

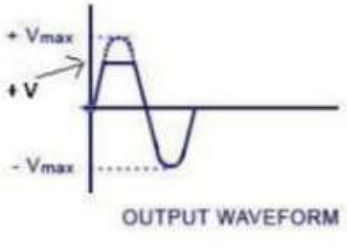
➢ BIASED POSITIVE CLIPPER

➢ When a small portion of the positive half cycle is to be removed, it is called a biased positive clipper. The circuit diagram and waveform is shown in the figure below.

BIASED POSITIVE CLIPPER







➢ During negative half cycle, when the input signal voltage is negative, the diode 'D' is reverse-biased. This causes it to act as an open-switch. Thus the entire negative half cycle appears across the load, as illustrated by output waveform.

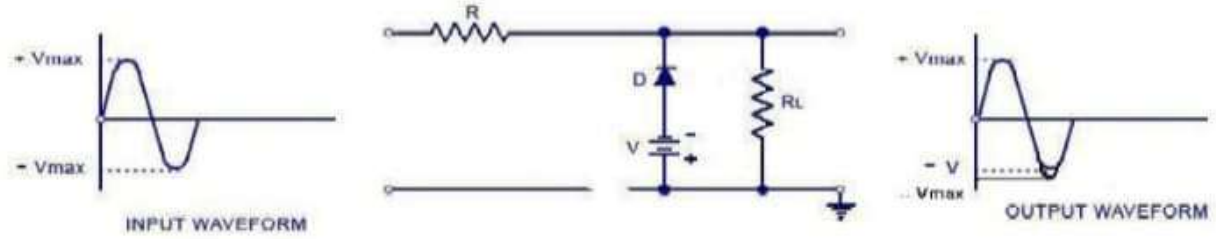
➢ During positive half cycle, when the input signal voltage is positive but does not exceed battery the voltage 'V', the diode 'D' remains reverse-biased and most of the input voltage appears across the output.

- When during the positive half cycle of input signal, the signal voltage becomes more than the battery voltage V, the diode D is forward biased and so conducts heavily. The output voltage is equal to '+ V' and stays at '+ V' as long as the magnitude of the input signal voltage is greater than the magnitude of the battery voltage, 'V'.
- Thus a biased positive clipper removes input voltage when the input signal voltage becomes greater than the battery voltage.

BIASED NEGATIVE CLIPPER

- When a small portion of the negative half cycle is to be removed, it is called a biased negative clipper. The circuit diagram and waveform is shown in the figure below.

BIASED NEGATIVE CLIPPER

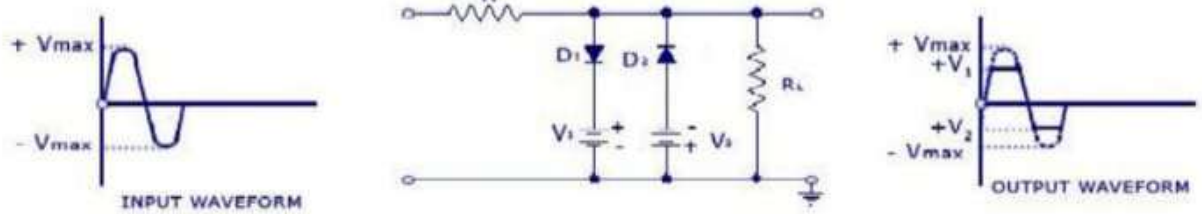


- During positive half cycle, when the input signal voltage is positive, the diode 'D' is reverse-biased. This causes it to act as an open-switch. Thus the entire positive half cycle appears across the load, as illustrated by output waveform.
- During negative half cycle, when the input signal voltage is negative but does not exceed battery the voltage 'V', the diode 'D' remains reverse-biased and most of the input voltage appears across the output.
- When during the negative half cycle of input signal, the signal voltage becomes more than the battery voltage V, the diode D is forward biased and so conducts heavily. The output voltage is equal to '-V' and stays at '-V' as long as the magnitude of the input signal voltage is greater than the magnitude of the battery voltage, 'V'.
- Thus a biased negative clipper removes input voltage when the input signal voltage becomes greater than the battery voltage.

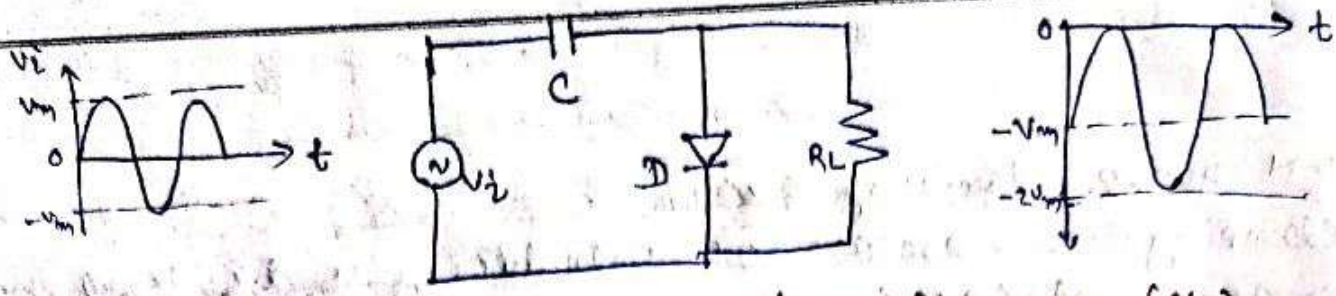
COMBINATION CLIPPER:-

- Combination clipper is employed when a portion of both positive and negative of each half cycle of the input voltage is to be clipped (or removed) using a biased positive and negative clipper together. The circuit for such a clipper is given in the figure below.

COMBINATION CLIPPER



- For positive input voltage signal when input voltage exceeds battery voltage $+V_1$ diode D_1 conducts heavily while diode D_2 is reversed biased and so voltage $+V_1$ appears across the output. This output voltage $+V_1$ stays as long as input signal voltage exceeds $+V_1$.
- On the other hand for the negative input voltage signal, the diode D_1 remains reverse biased and diode D_2 conducts heavily only when input voltage exceeds battery voltage V_2 in magnitude.
- Thus during the negative half cycle the output stays at $-V_2$ so long as the input signal voltage is greater than $-V_2$.



(i/p) (Negative clamper) (o/p)

CP-2 Special semiconductor Devices

Thermistor -:

* Thermistor is a combination of thermal & resistor. (thermally sensitive resistor)
* It is a type of resistor whose resistance is dependent on temperature. Used -: as temp. sensor. ex- fire alarms, ovens and refrigerators.
* Classification of thermistors in terms of temp. coefficient of resistance -:

a) Positive temp. coefficient (PTC) thermistors -:
→ They have positive temp. coefficient of resistivity. (the resistance increases as temperature increases).

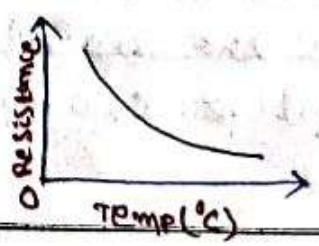
b) Negative temp. coefficient (NTC) thermistors -: ex- Fluorescent lamp.
→ They have negative temp. coefficient of resistivity. (the resistance decreases as temp. increases)
ex-: Air conditioners, refrigerators etc.

* Most thermistors have a negative temp. coefficient.
* The reason of NTC of a thermistor is that when its temp. is increased, the concentration of charge carriers (free electrons & holes) also increases which results a decrease in resistance.
* Resistance value of thermistor -: 100 Ω to 10 mega ohm.

Characteristic of thermistor -:

a) Resistance vs temp. characteristics

$$R = R_0 \alpha e^{\beta/T}$$



Where -: α & β = Constant

R_0 = Resistance at 0°C. , T = Temp.

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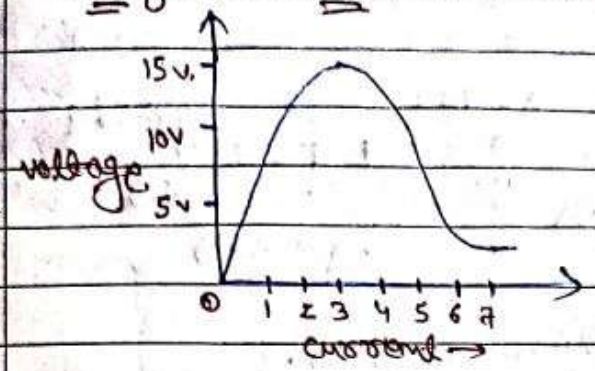
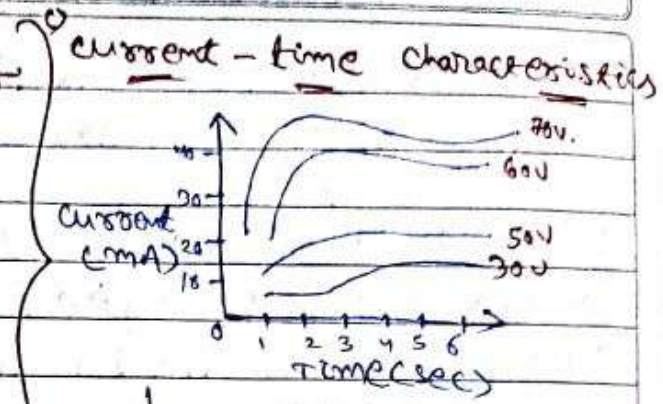
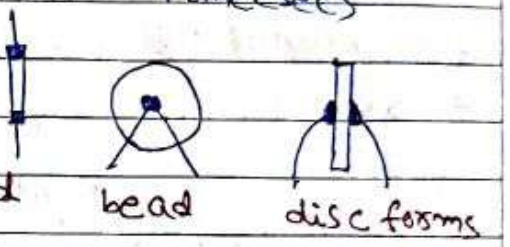
b) Voltage - current characteristics:-



Current - time characteristics



Sensistor:-



* It is a heavily doped bulk semiconductor which has positive temperature coefficient of resistance.
(Bulk semiconductor:- It is a single semiconductor crystal, appropriately doped & provided with ohmic contacts (junction) at either end.)
* When the temp. of a sensistor is increased, the mobility of charge carriers is decreased & hence the resistivity is increased.
* Resistance value of sensistor:- 0.7% per degree C over the temp. range of -60 to +150°C.

Application:-

i) It is used in an electronic circuit.
ii) It is used as temp. sensor for electronic thermometer
iii) It is used as a thermal relay.

*(Thermal relay:- It is a protector that uses the thermal effect of current to cut off the circuit.)

Barretter:-

→ A barretter have a positive temp. coefficient of resistance.

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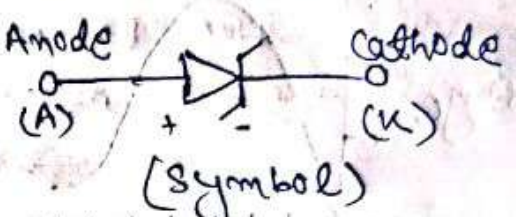
→ It is used to measure or detect power at radio, microwave and optical frequencies.

→ Power range :- 10^{-5} mW to 20mW.

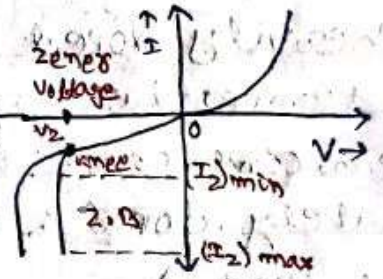
Zener Diode :-



(Symbol)

* Zener diode is a reverse biased heavily-doped (silicon) P-N junction diode which is operated in the breakdown region.
* Due to higher temp. & current capability, Silicon is preferred over germanium.

V-I Characteristics :-



Zener diode specifications

a) Zener voltage (V_Z) :-
→ This is the reverse voltage across the zener diode at which the reverse current increases sharply.

b) Maximum power dissipation (P_Z) :-

$$P_Z = V_Z \times I_Z$$

V_Z = Zener voltage.
I_Z = Reverse current.

c) Zener resistance (r_Z) :-

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

Application :-

a) Voltage regulation.
b) Switching operation.
c) Meter protection.

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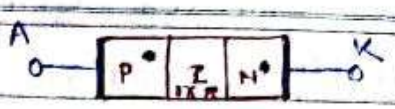
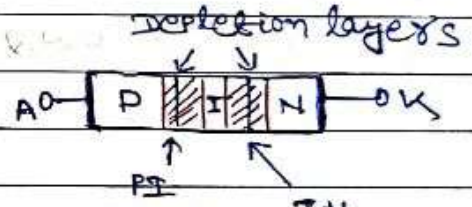
PIN Diode :-



* It is otherwise known as positive - Intrinsic - Negative diodes.
* In this diode, a high resistivity intrinsic layer is sandwiched between P+ and N+ regions.
* Due to increased separation between P and N regions, the capacitance decreases.
* So PIN diode has ~~faster~~ response time as compared to PN diode (switching time) & are useful at high frequency.
* I layer has a resistivity of 10 Ω-cm.
* When a PIN diode is forward biased, it offers a variable resistance and when it is reversed biased, it offers infinite resistance.

Working :- Bias condn.

Case-1) (No voltage / Current)



* With no bias applied, ~~there will~~ A diffusion of charge carriers take place across the junction.
* The diffusion of electrons and holes produce a depletion layer across PI and IN junction.
* The depletion layers penetrate to a little distance in P and N regions while a larger distance in I region. Thus, the device has a high value of resistance.

Case-2) Forward biased (Vbg condn)

* When ~~forward~~ biased voltage is applied, charge carrier inject into I layer from P and N region and reduces its forward resistance. (Depletion layer decreases)
* Thus, when a PIN diode is forward biased, it acts like a variable resistance.
* Resistance value :- 0.5 to 10 Ω

Teacher's Signature : _____

Case-3 (Reverse biased condn) -:

* when reverse bias voltage is applied, the depletion layer gradually increased & become more thick until the entire I region is swept free of charge carriers.
* This voltage is called as swept out voltage & PIN diode is act like a constant capacitance.
* Resistance value -: 5 to 10KΩ

Application -:

1. It can be used as an alternator.
2. It is used as constant impedance device.
3. PIN diode can be used in construction of phase modulator & amplitude modulator.
4. It can be used as phase shifter.
5. It can be used as T-R switch in radar applications.

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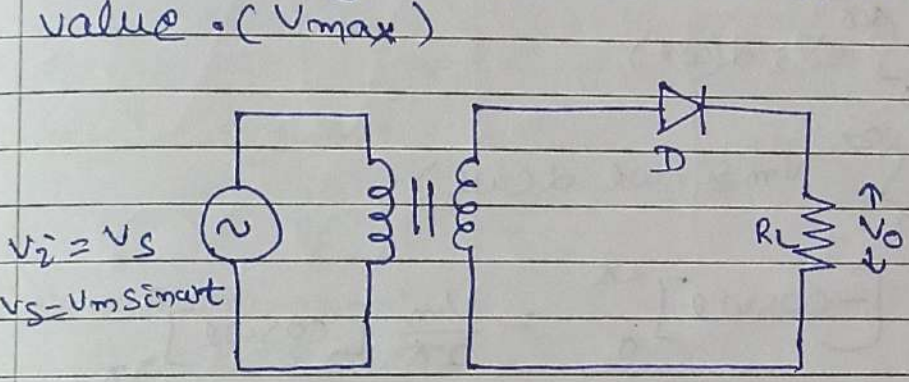
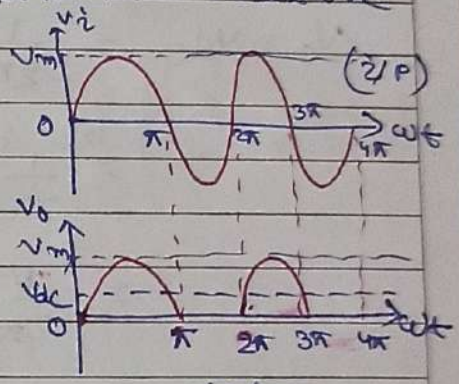
Half-wave Rectifier (uncontrolled)

* A rectifier is defined as an electronic device used for converting A.C voltage or current into d.c voltage or current. (unidirectional voltage or current)
* A halfwave rectifier is one which converts A.C voltage into a pulsating voltage using only one half cycle of the applied A.C voltage.
* Pulsating DC voltage :- It is a DC voltage whose value changes between '0' & a maximum positive value. (V_{max})



(circuit diagram)



(O/P)

(waveform)

* In this circuit, we used a Diode (D) connected in series with the load resistor (R_L).
* Here a transformer is used for step up or step down the input voltage.

Working :-

* Case -(1) $(0 \leq \omega t \leq \pi)$ [+ve half cycle]

→ During +ve half cycle, the diode (D) is forward biased & hence it conducts.

→ Thus, current is flowing in the circuit & we can found the output voltage & output current at the load side.

→ Here, voltage drop across diode is '0'. $(V_D = 0)$

Teacher's Signature :

Case-(2) ($\pi \le \omega t \le 2\pi$) (-ve half cycle)

* For negative half cycle, the diode (D) is reversed biased and hence it does not conduct.
* So, no current is flowing through the ckt. i.e. $V_0 = 0$, $i_0 = 0$.
* Here, the voltage drop across the diode is equal to the supply voltage. ($V_D = V_S$)

Analysis -:

a> D.C output voltage -:

$$V_0 = V_{dc} = \frac{1}{2\pi}\int_0^{\pi} V_i \, d(\omega t)$$

$$= \frac{1}{2\pi}\int_0^{\pi} V_m \sin\omega t \, d(\omega t)$$

$$= \frac{V_m}{2\pi}\left[-\cos\omega t\right]_0^{\pi} = \frac{V_m}{2\pi}\left[\cos\omega t\right]_{\pi}^{0}$$

$$= \frac{V_m}{2\pi}\left[1-(-1)\right] = \frac{V_m}{2\pi} \times 2 = \frac{V_m}{\pi}$$

$$\therefore \boxed{V_0 = V_{dc} = \frac{V_m}{\pi} = 0.318 V_m}$$

b> D.C output current -:

$$\boxed{i_0 = i_{dc} = \frac{V_{dc}}{R_L} = \frac{V_m}{\pi R_L} = 0.318\frac{V_m}{R_L}}$$

c> R.M.S. voltage -:

$$V_{RMS} = \left[\frac{1}{2\pi}\int_0^{\pi} V_i^2 \, d(\omega t)\right]^{1/2}$$

(V_{ac})

$$= \left[\frac{1}{2\pi}\int_0^{\pi} V_m^2 \cdot \sin^2\omega t \, d(\omega t)\right]^{1/2}$$

$[\cos 2x = 1 - 2\sin^2 x]$

$\Rightarrow \left[\sin^2 x = \frac{1-\cos 2x}{2}\right]$

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$$= \left[\frac{V_m^2}{2\pi}\int_0^{\pi}\left\{\frac{1-\cos 2\omega t}{2}\right\} d(\omega t)\right]^{1/2}$$

$$= \left[\frac{V_m^2}{4\pi}\left[\omega t - \frac{\sin 2\omega t}{2}\right]_0^{\pi}\right]^{1/2}$$

$$= \frac{V_m}{2}\left[\frac{1}{\pi}\left[(\pi-0) - \left(\frac{\sin\pi}{2}^{0} - \frac{\sin 0}{2}^{0}\right)\right]\right]^{1/2}$$

$$= \frac{V_m}{2}\left[\frac{1}{\pi}\times\pi\right]^{1/2} = \frac{V_m}{2}$$

d) RMS current -:

$$i_{RMS} = \frac{V_{RMS}}{R} = \frac{V_m}{2R}$$

e) Form factor -: (F)

$$F = \frac{\text{RMS value}}{\text{Avg. value}} = \frac{V_m/2}{V_m/\pi} = 1.57$$

f) Peak factor -:

$$\text{Peak factor} = \frac{\text{Peak value}}{\text{R.M.S value}} = \frac{V_m}{V_m/2} = 2$$

g) Peak inverse voltage (PIV)

→ It is defined as the maximum voltage across the diode in the reverse direction. (V_m)

h) Rectifier efficiency -:

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{0.3+8}{0.5} \frac{V_m}{V_m} \quad \frac{\frac{V_m^2}{\pi^2}\times R_L}{\frac{V_m^2}{4}\times R_L} = \frac{4}{\pi^2}$$

$$P_{dc} = (V_{dc})^2 \times R_L = \frac{V_m^2}{\pi^2}\times R_L \qquad = 0.406$$

$$P_{ac} = \frac{V_m^2}{4}\times R_L \qquad = 40.6\%$$

Teacher's Signature :

i) Ripple factor (γ)

$$= \sqrt{F^2-1} = \sqrt{1.57^2-1} = 1.21$$

i) Ripple factor Tapping:- the connection point along the T/F winding to select the suitable no. of turns.

$$\gamma = \frac{\text{ripple voltage}}{\text{d.c. voltage}} = \frac{V_{RMS}}{V_{dc}} = \frac{V_m/2}{V_m/\pi}$$

Fullwave Rectifier :-

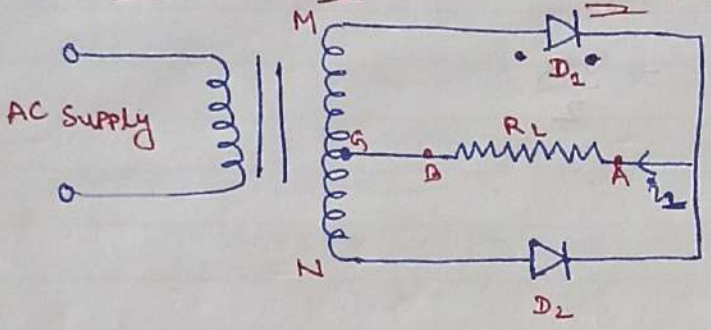
* In fullwave rectifier, both half cycle of the input are utilized with the help of two diodes working alternately.

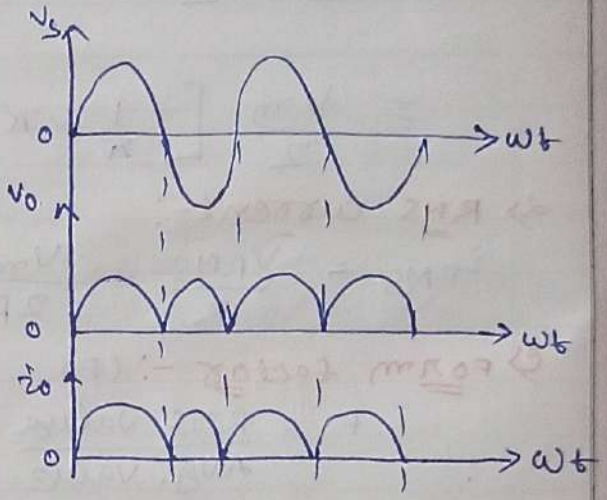
→ It is of two type.

a) center tapped rectifier

b) Bridge Rectifier.

center tapped Rectifier :-





working :-

* when input A.C supply is switched on, the ends M and N of the transformer secondary becomes positive and negative alternately.
* During +ve half cycle, terminal M is +ve, G is at zero potential & N is at negative potential.
* At that time, Diode (D_1) is forward biased & conducts, causes a current (i_1) is flowing through the load & Diode
* D_2 is reversed biased & off condition.
* During -ve half cycle, terminal N is +ve, G is at zero potential & M is at negative potential.
* At that time, Diode (D_2) is forward biased & conducts, But Diode (D_1) is reversed biased & off condition.

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* During this condition, current (i_2) is flowing through the load resistance (R_L).

Note :- current flowing path :-

+ve half cycle :- ('M' terminal - D_1 - R_L - G terminal)

-ve half cycle :- ('M' terminal - D_2 - R_L - G terminal)

* In both the cases, the current flows direction is same. (A to B direction)

Analysis :-

a) D.C output voltage :-

$$V_o = V_{dc} = \frac{1}{\pi}\int_0^{\pi} V_m \sin\omega t \, d(\omega t)$$

$$= \frac{V_m}{\pi}\left[-\cos\omega t\right]_0^{\pi} = \frac{V_m}{\pi}\left[\cos\omega t\right]_{\pi}^{0}$$

$$= \frac{V_m}{\pi}\left[1-(-1)\right] = \frac{2V_m}{\pi} = 0.637\,V_m$$

b) D.C output current :-

$$i_o = i_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi R_L} = 0.637\,\frac{V_m}{R_L}$$

c) RMS voltage :-

$$V_{RMS} = V_{ac} = \left[\frac{1}{\pi}\int_0^{\pi} V_m^2 \sin^2\omega t \, d(\omega t)\right]^{1/2}$$

$$= \left[\frac{V_m^2}{\pi}\int_0^{\pi}\left(\frac{1-\cos 2\omega t}{2}\right).d(\omega t)\right]^{1/2}$$

$$= \left[\frac{V_m^2}{2\pi}\left[\omega t - \frac{\sin 2\omega t}{2}\right]_0^{\pi}\right]^{1/2}$$

$$= \left[\frac{V_m^2}{2\pi}\left[(\pi-0) - \left(\frac{\sin 2\pi}{2} - \frac{\sin 2\cdot 0}{2}\right)\right]\right]^{1/2}$$

$$= \left[\frac{V_m^2}{2\pi}\times\pi\right]^{1/2} = \frac{V_m}{\sqrt{2}} = 0.707\,V_m$$

Teacher's Signature :

d) RMS current :-

$$i_{RMS} = i_{ac} = \frac{V_{RMS}}{R_L} = \frac{V_m}{\sqrt{2} R_L} = 0.707 \frac{V_m}{R_L}$$

e) Rectifier Efficiency :-

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{4V_m^2}{\pi^2 R_L} \Big/ \frac{V_m^2}{2R_L} = \frac{8}{\pi^2} = 0.812 = 81.2\%$$

$$P_{dc} = \frac{V_{dc}^2}{R_L} = \frac{\left(\frac{2V_m}{\pi}\right)^2}{R_L} = \frac{4V_m^2}{\pi^2 R_L}$$

$$P_{ac} = \frac{V_{ac}}{R_L} = \frac{\left(\frac{V_m}{\sqrt{2}}\right)^2}{R_L} = \frac{V_m^2}{2R_L}$$

f) Peak inverse voltage (PIV) ($2V_m$)

g) Form factor :- (F)

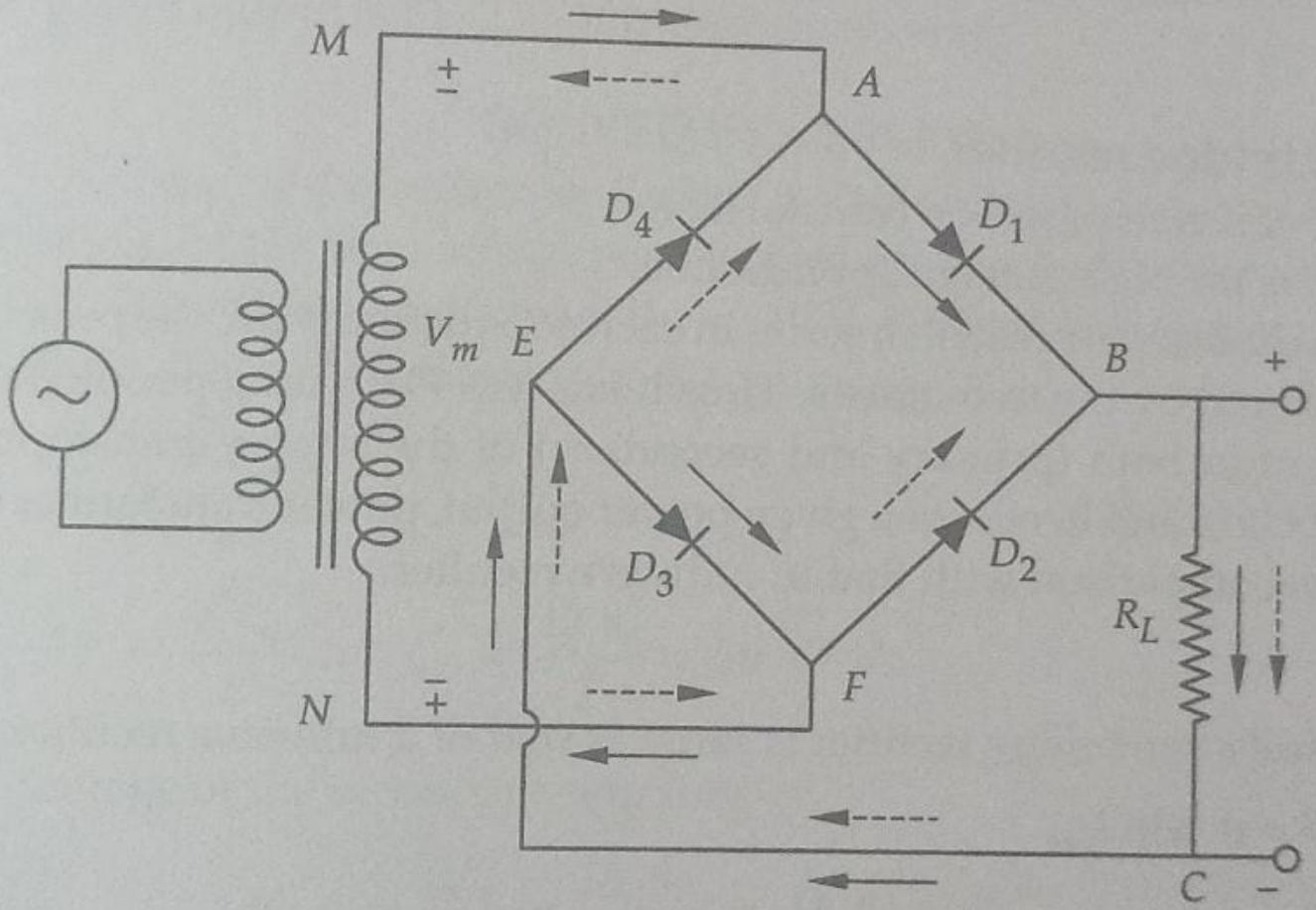
$$f = \frac{\text{RMS value}}{\text{Avg. o/p value}} = \frac{V_m/\sqrt{2}}{2V_m/\pi} = \frac{1}{\sqrt{2}} \times \frac{\pi}{2} = 1.11$$

h) Peak factor :- $\frac{\text{Peak value}}{\text{RMS value}} = \frac{V_m}{V_m/\sqrt{2}} = \sqrt{2}$

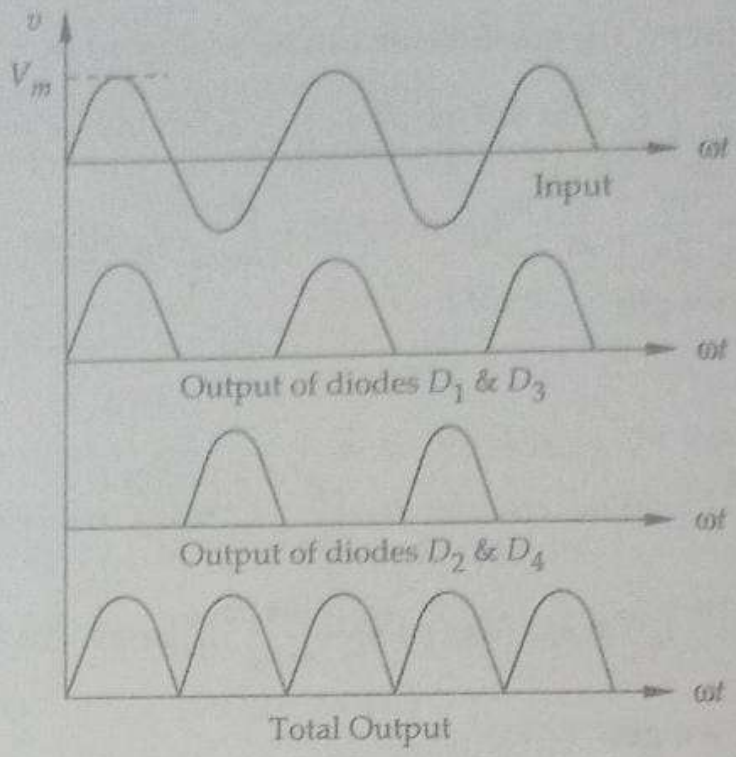
i) Ripple factor :- $\sqrt{F^2 - 1} = \sqrt{(1.11)^2 - 1} = 0.48$

8.4 FULL-WAVE BRIDGE RECTIFIER

A circuit frequently used for electronic d.c. power supplies is a fullwave bridge rectifier. In fullwave bridge rectifier four diodes are used as shown in fig. (8·13).



(a) Fullwave bridge rectifier circuit



(b) Output waveform

Fig. 8·13

During the positive input half cycle, terminal M of the secondary of the transformer is positive while the terminal N is negative. In this situation diodes D_1 and D_3 are forward biased (ON position) *i.e.*, they conduct where as diodes D_2 and D_4 are reversed biased (OFF position) *i.e.*, they do not conduct. So a current flows along *MABCEFN* as shown by arrow in fig. [8·13 (a)]. There will be a voltage drop across R_L.

During the negative input half cycle, terminal N of the secondary of transformer becomes positive while the terminal M becomes negative. Under this situation diodes D_2 and D_4 are forward biased (ON position) *i.e.*, they conduct whereas diodes D_1 and D_3 are reversed biased (OFF position) *i.e.*, they do not conduct. Now a current flows along *NFBCEAM* as shown by dotted arrow in fig. [8·13 (a)]. The current produces a voltage drop across R_L.

It is obvious from the figure that current through load resistance R_L is in the same direction *AB* during both half cycle of the input a.c. supply. The output waveforms are shown in fig. [8·13 (b)]. Here, the waveform of the load current is essentially the same as in case of a fullwave rectifier.

Advantages of bridge rectifier

(i) No centre-tap is required on transformer.

(ii) It is suitable for high voltage applications.

(iii) Since two diodes are present in series in each conduction path, the peak inverse voltage is equally shared by the two diodes. Thus it has less PIV rating per diode.

(iv) The current in both (primary and secondary) of the supply transformer flows for the entire a.c. cycle and hence for a given power output, power transformer of small size may be used in comparison with that in fullwave rectifier.

❖ FILTER CIRCUITS:-

- Generally, a rectifier is required to produce pure D.C. supply for using at various places in the electronic circuits.
- However, the output of a rectifier has pulsating character i.e. it contains A.C. and D.C. components.
- The A.C. component is undesirable and must be kept away from the load.
- To do so, a filter circuit is used which removes (or filters out) the A.C. component and allows only the D.C. component to reach the load.
- A **filter circuit** is a device which removes the A.C. component of rectifier output but allows the D.C. component to reach the load.
- A filter circuit is generally a combination of inductors (L) and capacitors (C).
- The filtering action of L and C depends upon the basic electrical principles.
- A capacitor offers infinite reactance to d.c.
- We Know that $X_C = 1/2\pi fC$. But for D.C., $f = 0$.

  $\therefore$ $X_C = 1/2\pi fC = 1/ 2\pi \times 0 \times C = \infty$ (Means Capacitor shows *infinite reactance* to DC)

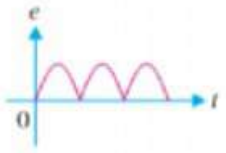
  ♣ ***Hence, a Capacitor does not allow d.c. to pass through it.***

- We know $X_L = 2\pi fL$. For d.c., $f = 0$

  $\therefore$ $X_L = 2\pi \times 0 \times L = 0$ (Means Inductor shows *zero reactance* to DC)

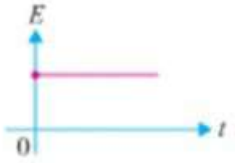
  ♣ ***Hence Inductor passes d.c. quite readily.***

- *A Capacitor passes A.C. but does not pass D.C. at all. On the other hand, an Inductor opposes A.C. but allows D.C. to pass through it.*
- It then becomes clear that suitable network of L and C can effectively remove the A.C. component, allowing the D.C. component to reach the load.



(Pulsating D.C)

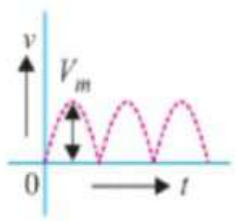
(Filter Circuit)



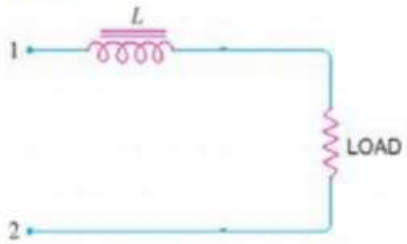
(Pure D.C)

- **Types Of Filter Circuits:-**
- There are different types of filter circuits according to their construction. The most commonly used filter circuits are : -
  - ♣ *Inductive Filter or Series Inductor,*
  - ♣ *Capacitor Filter or Shunt Capacitor,*
  - ♣ *Choke Input Filter or LC Filter* and
  - ♣ *Capacitor Input Filter* or *π-Filter*.

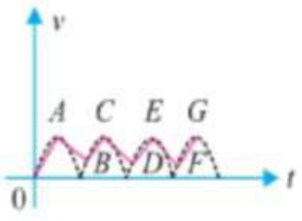
✓ Inductive Filter Or Series Inductor:-



(Rectified output Pulsating d.c)



(Inductive Filter Circuit)

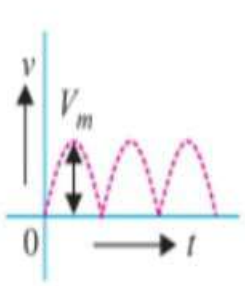


(Output of Inductive Filter)

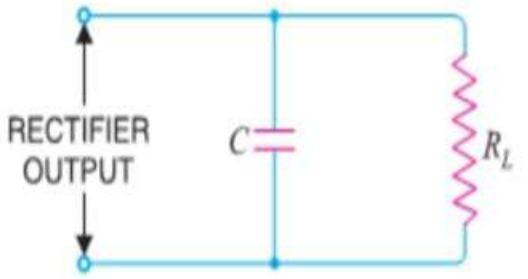
- Fig. (ii) Shows a typical Inductive filter circuit. It consists of an Inductor L placed across the rectifier output in series with load R_L.

- The choke (Inductor with iron core) offers high opposition to the passage of a.c. component but no opposition to the d.c. component.
- The result is that most of the a.c. component appears across the choke while whole of d.c. component passes through the choke on its way to load. This results in the reduced pulsations at Load resistance R_L.

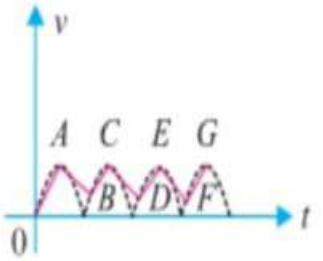
✓ **Capacitor Filter Or Shunt Capacitor:-**



(Rectified output Pulsating d.c)



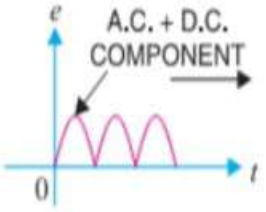
(Capacitor Filter Circuit)



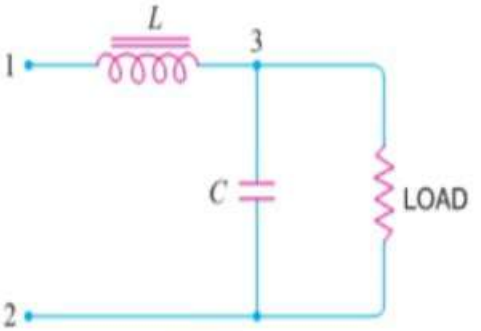
(Output of Capacitor Filter)

- Fig. (ii) Shows a typical capacitor filter circuit. It consists of a capacitor C placed across the rectifier output in parallel with load R_L.
- The pulsating direct voltage of the rectifier is applied across the capacitor. As the rectifier voltage increases, it charges the capacitor and also supplies current to the load.
- At the end of quarter cycle [Point A in Fig. (iii)], the capacitor is charged to the peak value V_m of the rectifier voltage.
- Now, the rectifier voltage starts to decrease. As this occurs, the capacitor discharges through the load and voltage across it decreases as shown by the line AB in Fig. (iii).
- The voltage across load will decrease only slightly because immediately the next [illegible] and recharges the capacitor.
- This process is repeated again and again and the output voltage waveform becomes ABCDEFG. It may be seen that very little ripple is left in the output.
- Moreover, output voltage is higher as it remains substantially near the peak value of rectifier output voltage.
- The capacitor filter circuit is extremely popular because of its low cost, small size, little weight and good characteristics.

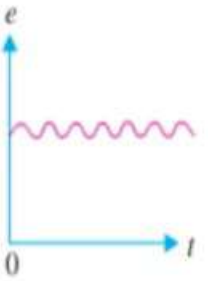
✓ **Choke Input Filter Or LC Filter:-**



(Rectified output Pulsating d.c)



(Choke Input Filter Circuit)

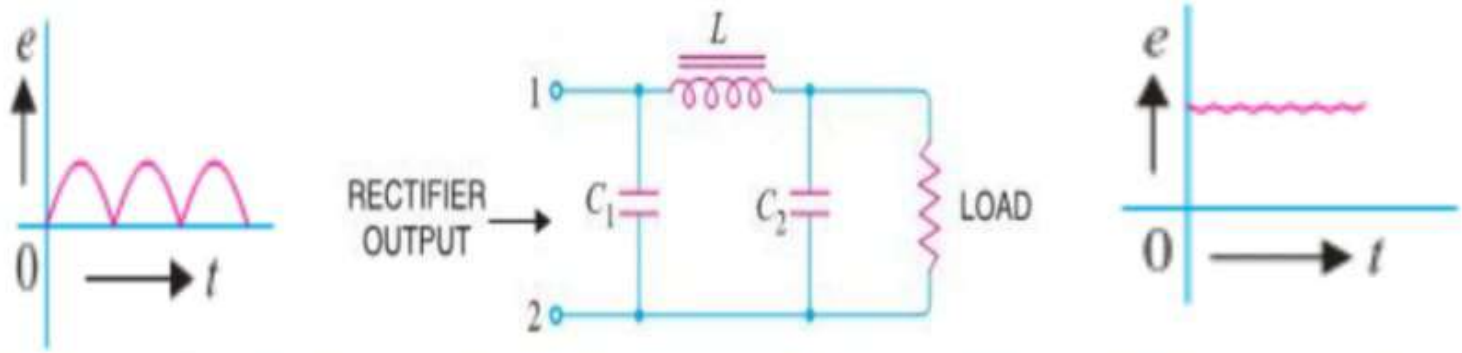


(Output of Choke Input Filter)

- Fig. shows a typical choke input filter circuit. It consists of a choke L connected in series with the rectifier output and a filter capacitor C across the load.
- Only a single filter section is shown, but several identical sections are often used to reduce the pulsations as effectively as possible.
- The pulsating output of the rectifier is applied across terminals 1 and 2 of the filter circuit.
- As discussed before, the pulsating output of rectifier contains a.c. and d.c. components. The choke offers high opposition to the passage of a.c. component but negligible opposition to the d.c. component.
- The result is that most of the a.c. component appears across the choke while whole of d.c. component passes through the choke on its way to load. This results in the reduced pulsations at terminal 3.

- At terminal 3, the rectifier output contains d.c. component and the remaining part of a.c. component which has managed to pass through the choke.
- Now, the low reactance of filter capacitor bypasses the a.c. component but prevents the d.c. component to flow through it. Therefore, only d.c. component reaches the load.
- In this way, the filter circuit has filtered out the a.c. component from the rectifier output, allowing d.c. component to reach the load.

✓ **Capacitor Input Filter or π-Filter:-**



(Rectified output Pulsating d.c) (Capacitor Input or π- Filter Circuit) (Output of π-Filter)

- Fig. shows a typical capacitor input filter or π-filter. It consists of a filter capacitor C_1 connected across the rectifier output, a choke Lin series and another filter capacitor C_2 connected across the load.
- Only one filter section is shown but several identical sections are often used to improve the smoothing action. The pulsating output from the rectifier is applied across the input terminals (i.e. terminals 1 & 2) of the filter.
- The filtering action of the three components viz C_1 , L and C_2 of this filter is described below :

  (a) The **filter capacitor C_1** offers low reactance to a.c. component of rectifier output while it offers infinite reactance to the d.c. component. Therefore, capacitor C_1 bypasses an appreciable amount of a.c. component while the d.c. component continues its journey to the choke L.

  (b) The **choke L** offers high reactance to the a.c. component but it offers almost zero reactance to the d.c. component. Therefore, it allows the d.c. component to flow through it, while the un bypassed a.c. component is blocked.

  (c) The **filter capacitor C_2** bypasses the a.c. component which the choke has failed to block. Therefore, only d.c. component appears across the load and that is what we desire

Transistor

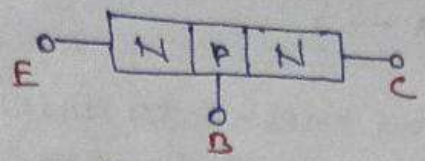
* Transistor = Trans + istor
→ Trans means the signal transfer property of the device.
→ istor means a solid element like resistors.
* A transistor is basically a solid state semiconductor device which acts like a switch and an amplifier.
* It also used to control or regulate the flow of electronic signals.
→ The weak signal is introduced in the low resistance circuit & output is taken from the high resistance. Therefore, a transistor transfers a signal from a low resistance to high resistance.
→ It is of two type a) BJT - Bipolar junction transistor
b) FET - Field effect transistor.

Bipolar Junction transistor (BJT)

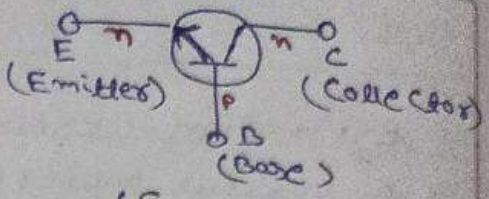
→ A BJT is a type of transistor that used both the charge carriers (electrons & holes) for the current conduction.
→ It is of two type. a) N-P-N transistor.
b) P-N-P transistor.
→ BJT has 3 terminals (Emitter (E), Base (B), Collector (C) & 2 junction.

Teacher's Signature : _____

NPN transistor :-



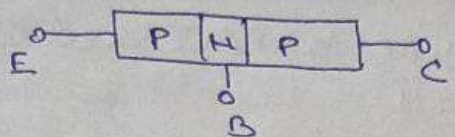
(Structure) diagram



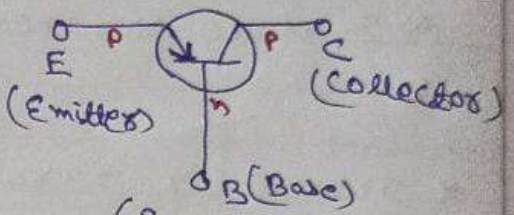
(Symbol) diagram.

→ When a layer of 'P' type semiconductor is sandwiched between two layer of 'N' type semiconductor, then NPN transistor will form.

PNP transistor :-



(structure) diagram.



(Symbol)

→ When a layer of 'N' type semiconductor is sandwiched between two layer of 'P' type semiconductor, then PNP transistor will form.

Note :- A transistor has two PN junction, one junction is forward biased & the other is reverse biased.

→ The forward biased junction has a low resistance path where as a reverse biased junction has a high resistance path.

Transistor terminals :-

→ A transistor has three section of doped semiconductors.

→ The section on one side is the emitter and the section on the opposite side is the collector.

→ The middle section is called the base & forms two junction between the emitter & the collector.

i> Emitter :- This forms the left hand section or region of the transistor.

→ The main function of this region is to supply majority charge carriers (either electrons or holes) to the base.

→ Hence, it is heavily doped in comparison to other regions.
→ The arrowhead is always indicates the conventional direction of current flow & always located on the emitter terminal.
→ The emitter is always forward biased w.r.t base so that it can supply a large no. of majority carriers.
→ In case of N-P-N transistor it is from base to emitter (base is +ve w.r.t emitter), while in case of P-N-P transistor, it is from emitter to base (emitter is +ve w.r.t base)

Base -: The middle section of the transistor is known as base.

→ This is very lightly doped & is very thin (10^{-6}m) as compared to either emitter or collector. So that it may pass most of the injected charge carriers to the collector.

Collector -: The right hand section of the transistor is called as collector.

→ The main function of the collector is to collect majority charge carriers through the base.
→ This is moderately doped.
→ The collector is always Reversed biased w.r.t base & it offer high resistance.
→ In most of the transistors, the collector region is made physically larger than the emitter region. This is due to the fact that collector has to dissipate much greater power.
→ Due to this difference, collector & emitter are not interchangeable.

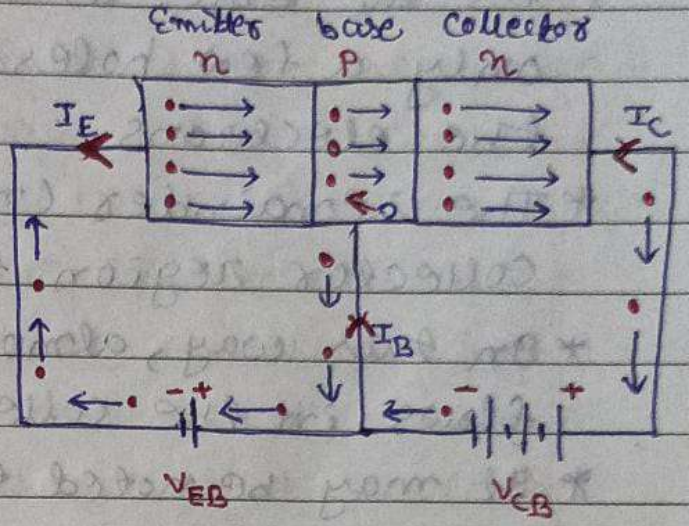
thickness	wide	thin	wider
doping level	Heavily dope (Emitter)	lightly doped (Base)	Moderately doped. (Collector)

Teacher's Signature:

Transistor Action :-

Working of NPN transistor :-

* In this circuit diagram, the npn transistor with forward biased to Emitter-base junction & reverse biased to collector-base junction.

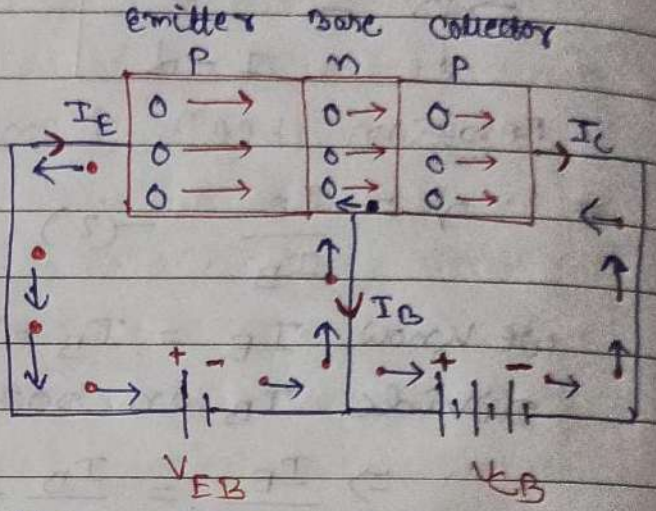


* The forward bias causes the electrons in the n-type emitter to flow towards the base.
* As these electrons flow through the P-type base, they tend to combine with holes.
* As the base is lightly doped and very thin, therefore, only a few electons (less than 5%) combine with holes to constitute base current I_B.
* The remainder (more than 95%) cross over into the collector region to constitute collector current I_C.
* In this way, almost the entire emitter current flows in the collector circuit & the current conduction in NPN transistor is carried out by electron.

So $\boxed{I_E = I_B + I_C}$

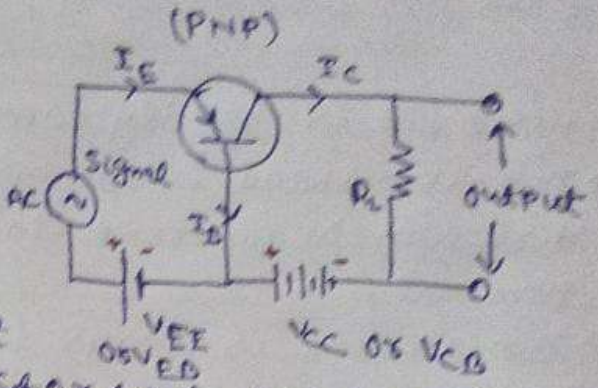
Constitue -: Be a part of

Working of PNP transistor -:



* This circuit diagram shows the basic connection of a PNP transistor.
* The forward bias causes the holes in the P-type emitter to flow towards the base.
* This constitutes the emitter current I_E.
* As these holes cross into n-type base, they tend to combine with the electrons.
* As the base is lightly doped & very thin, therefore only a few holes (less than 5%) combine with the electrons.
* The remainder (more than 95%) cross into the collector region to constitute collector current I_C.
* In this way, almost the entire emitter current flows in the collector circuit.
* It may be noted that current conduction within PNP transistor is by holes. However, in the extral connecting wires, the current is still by electrons.

TRANSISTOR AS AN AMPLIFIER :-



→ This figure show the basic circuit diagram of a transistor amplifier.

→ Here, the weak signal to be amplified is applied between emitter-base circuit & the output is taken across the load resistor (R_L) connected in the collector circuit.

→ A d.c voltage (V_{EE}) is connected to the input side along with 'AC' signal & another dc voltage (V_{CC}) is connected to the output side. (Note :- $V_{CC} > V_{EE}$)

V_{EE} & V_{EB} :- Emitter base voltage.

V_{CC} & V_{CB} :- Collector base voltage.

→ If we don't connect (V_{EE}), then only the 'AC' signal will work. But we know that the emitter-base junction is always forward biased. So it don't work during negative half cycle of AC signal voltage.

→ Due to this region we used (V_{EE}) voltage source.

→ A small change in signal voltage produces an appreciable change in emitter current because the input circuit has low resistance.

→ Due to the transistor action, the change in emitter current causes almost the same change in collect current.

→ When the collector current flows through the load resistance (R_L), a large voltage is developed across it.

→ In this way, a weak signal applied in the input circuit appears in the amplified form across the output circuit.

→ If ΔV_o = Small output voltage change.

ΔV_i = Small input voltage change.

ΔI_E = Change in emitter current

ΔI_C = Change in collector current

α_{dc} = current amplification factor

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Thus $\alpha_{dc} = \frac{\Delta I_C}{\Delta I_E} \Rightarrow \Delta I_C = \alpha_{dc} \cdot \Delta I_E$ — (i)

Now, the change in output voltage across the load resistor

$\Delta V_0 = R_L \times \Delta I_C$ (ii)

$= R_L \times \alpha_{dc} \times \Delta I_E$ ($\because \Delta I_C = \alpha_{dc} \cdot \Delta I_E$)

then, the voltage amplification

$A = \frac{\Delta V_0}{\Delta V_i}$ — (iii)

If r_e = resistance of the emitter base junction

then $\boxed{\Delta V_i = r_e \times \Delta I_E}$ — (iv)

$\therefore A = \frac{\Delta V_0}{\Delta V_i} = \frac{R_L \times \alpha_{dc} \times \Delta I_E}{r_e \times \Delta I_E} \Rightarrow \boxed{A = \frac{\alpha_{dc} R_L}{r_e}}$ — (v)

Q// $r_e = 20\,\Omega$, $R_L = 100\,K\Omega$, AC signal (ΔV_i) = 400 mV, then Find voltage amplification (A). Assume $\alpha_{dc} = 1$.

Ans:- we know $\Delta V_i = r_e \cdot \Delta I_E$ • $\Delta V_i = 400mV$

$\Rightarrow 400 = 20 \times \Delta I_E$

$\Rightarrow \Delta I_E = \frac{400}{20} = 20mA$

then $\Delta I_C = \alpha \Delta I_E = 1 \times 20mA = 20mA$

output voltage $\Delta V_0 = \Delta I_C \times R_L = 20mA \times 100K\Omega$

$= 20 \times 10^{-3} \times 100 \times 10^{3} = 2000V.$

$\therefore$ voltage amplification (A) $= \frac{\Delta V_0}{\Delta V_i} = \frac{2000}{400 \times 10^{-3}} = \frac{2000 \times 10^{3}}{400} = 5000$ (Ans)

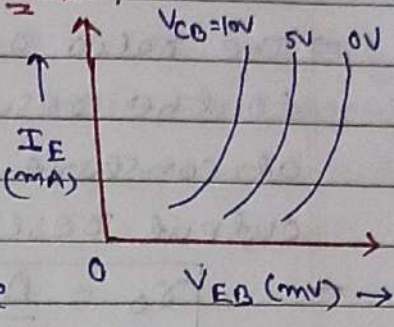
AE& OPAMP

CP-4 (Transistor)

Characteristics of common Base circuit :-

Input Characteristics :-

→ The input characteristics curve is drawn between emitter current (I_E) and emitter base voltage (V_{EB}) at constant collector base voltage (V_{CB}).



(input characteristics)

→ The emitter current (I_E) increases rapidly with small increase in emitter-base voltage (V_{EB}). This shows that the input resistance is very small.

Input resistance (r_i) :-

→ The ratio of change in emitter-base voltage (ΔV_{EB}) to the resulting change in emitter-current (ΔI_E) at constant collector-base voltage (V_{CB}) is defined as input resistance.

$$r_i = \frac{\Delta V_{EB}}{\Delta I_E} \quad V_{CB} = \text{constant}.$$

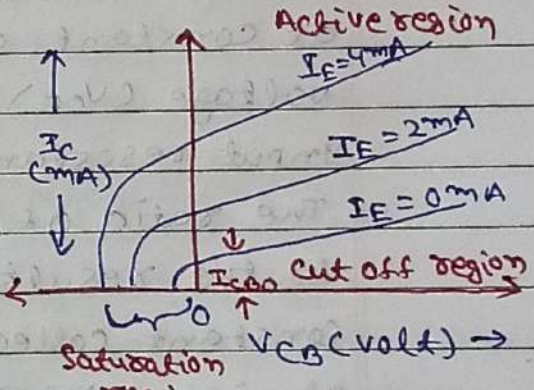
Output Characteristics :-

→ The output characteristics curve is drawn between collector current (I_C) and collector base voltage (V_{CB}) at constant emitter current (I_E).

→ In the active region (emitter junction is in forward biased & collector junction is in Reversed biased.

→ In the cut off region (when both emitter and collector junctions are reversed-biased), but a small amount of collector leakage current (I_{CBO}) is flow.

→ In the saturation region (when both emitter and collector junctions are forward biased.



(output characteristics)

I_{CBO} = Collector leakage current.

Output resistance -: (r_o)

→ The ratio of change in collector-base voltage (ΔV_{CB}) to the resulting change in collector current (ΔI_C) at constant emitter current (I_E) is defined as output resistance.

→ $$\boxed{r_o = \frac{\Delta V_{CB}}{\Delta I_C}} \quad I_E = \text{constant}.$$

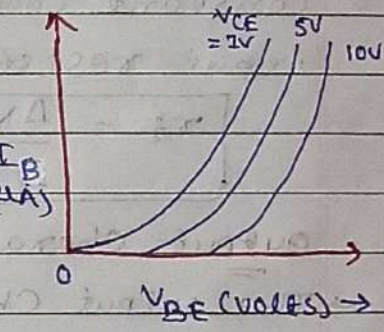
Q/ CB configuration, $\Delta V_{EB} = 200mV$, $\Delta I_E = 5mA$. Find r_i.

Ans-: $r_i = \frac{\Delta V_{EB}}{\Delta I_E} = \frac{200mA}{5mA} = 40\Omega$

Characteristics of Common Emitter Circuit -:

Input Characteristics -:

→ The input characteristics curve is drawn between base current (I_B) and base-emitter voltage (V_{BE}) at constant collector-emitter voltage (V_{CE}).



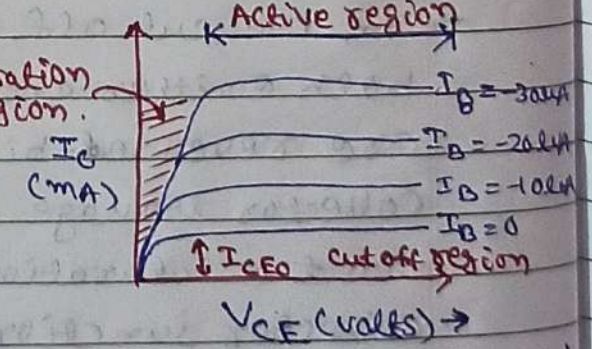
Input resistance -: (r_i)

→ The ratio of change in base emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage (V_{CE}) is defined as input resistance.

$$\boxed{r_i = \frac{\Delta V_{BE}}{\Delta I_B}} \quad V_{CE} = \text{Constant}.$$

Output Characteristics -:

→ The output characteristics curve is drawn between collector current (I_C) and collector emitter voltage (V_{CE}) at constant base current (I_B)



(Output characteristics)

Output resistance:- (r_o)

→ The ratio of change in collector-emitter voltage (ΔV_{CE}) to the resulting change in collector current (ΔI_C) at constant base current (I_B) is defined as output resistance.

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} \quad I_B = \text{constant}.$$

Q// A change of 300mV in base-emitter voltage causes a change of 100μA in the base current. Find the input resistance?

Ans:- $$r_i = \frac{\Delta V_{BE}}{\Delta I_B}\Big|_{V_{CE}=\text{constant}}$$

$$\Rightarrow r_i = \frac{300\times10^{-3}}{100\times10^{-6}} = 3\times10^3 = 3K\Omega \text{ (Ans)}$$

Q// Increase in collector emitter voltage from 5V to 8V. causes increase in collector current from 5mA to 5.3mA. Find the output resistance?

Ans:- $\Delta V_{CE} = 8-5 = 3V$, $\Delta I_C = 5.3-5 = 0.3\,mA$

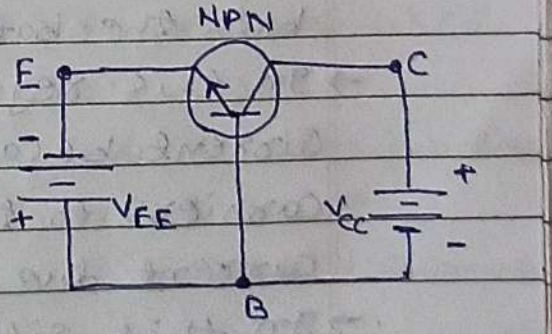
$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} = \frac{3}{0.3\times10^{-3}} = 10^4 = 10K\Omega \text{ (Ans)}$$

Different modes of operation of a transistor:-

Case	Emitter-base Junction(J_1)	Collector-base Junction	Region of operation
I	Forward-biased	Reverse-biased	Active
II	Forward-biased	Forward-biased	Saturation
III	Reverse-biased	Reverse-biased	Cut-off
IV	Reverse-biased	Forward-biased	Inverted

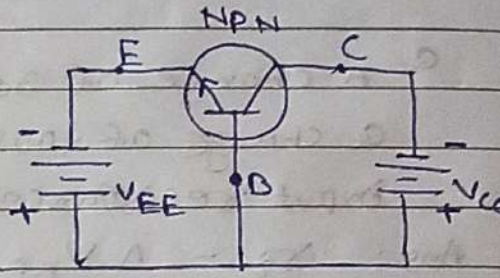
Case (I) Active Region:-

→ In this mode, the emitter-base junction is forward-biased while collector-base junction is reversed biased.



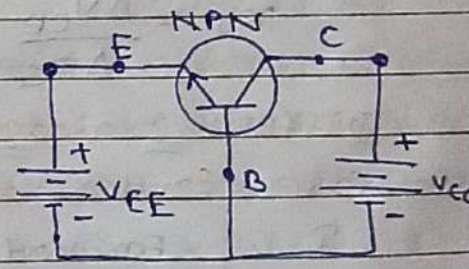
→ In the emitter-base circuit, a battery V_{EE} is connected such that negative of the battery is connected to emitter while positive is connected to base.
→ Similarly, a battery V_{cc} is connected to collector-base circuit. Positive terminal of battery is connected to collector while negative is connected to base.
→ In this region, the transistor is used for amplification.

Case (II) :- Saturation region :-



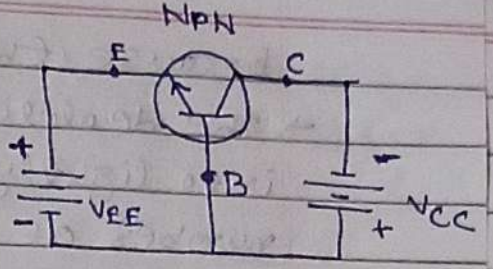
→ In this mode, emitter-base junction as well as collector base junction both are forward biased.
→ The negative of battery V_{EE} is connected to emitter and similarly the negative of battery V_{cc} is connected to collector. The positive terminals of both the batteries are connected to base.
→ In this case, the collector current becomes independent of base current. So, the transistor acts like a closed switch.

Case (III) Cut-off region :-



→ In this mode, both the junctions are reversed biased.
→ Here the positive of battery V_{EE} is connected to emitter & similarly the positive of battery V_{cc} is connected to collector. The negative terminals of both the batteries are connected to base.
→ In this region, the transistor has practically zero current because the emitter does not emit charge carriers to the base. Of course, there is negligibly current due to minority carrier. (leakage current)
→ In this situtiom, the transistor acts as open switch.

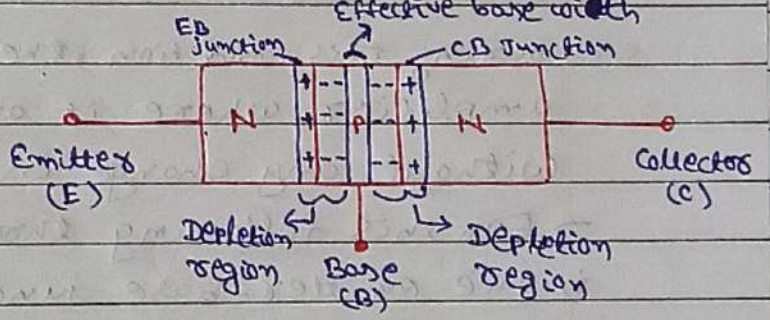
Case IV Inversed region



→ In this region, emitter-base junction is reversed-biased while collector-base junction is forward-biased.
→ In the emitter-base circuit, a battery V_{EE} is connected such that positive of the battery is connected to emitter while negative is connected to base.
→ Similarly, a battery V_{CC} is connected to collector-base circuit. Negative terminal of battery is connected to collector while positive is connected to base.
→ Here, the collector cannot inject the majority carriers into the base because the doping level of emitter and collector is not the same.
→ In this region, the action of transistor is very poor.

CP-5 Transistor Circuit

Unbiased Transistor :-



→ When no external supply is connected to a transistor, the transistor is said to be in unbiased condition.
→ A transistor is just like two diodes.
→ The junction betⁿ emitter and base may be called as emitter base diode or emitter diode.
→ Similarly, the junction between base and collector may be called as collector base diode or collector diode.
→ When no battery is connected between different terminals, the transistor is said to be unbiased or in open circuit state.
→ There are two depletion regions at the two junctions of a transistor.
→ The width of the two depletion layers will be different

because the regions are doped at different levels
→ The depletion region penetrates more deeply into lightly doped side so as to include an equal number of impurity atoms in each side of junction.
→ Therefore, the depletion region at emitter junction penetrates less in heavily doped emitter and extends more in base region.
→ Similarly, the depletion region at collector junction penetrates less in heavily doped collector and extends more in base region.
→ So, the depletion layer formed at collector junction is larger that depletion layer formed at emitter junction.

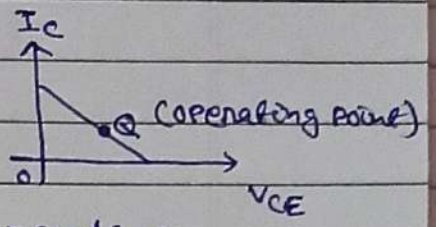
Transistor biasing :-
→ The process of Applying external d.c voltages across the different terminals of transistor is called Biasing.
→ During this condition, the transistor is works as an amplifier where it amplified the magnitude of signal without any change in shape.
→ For this following three conditions must be satisfied
i) The emitter-base junction should be forward biased.
ii) The collector-base junction should be Reverse biased.
iii) There should be proper zero signal collector current.
→ When a transistor is not properly biased, it works inefficiently and produces distortion in the output signal. Hence a transistor should be biased correctly.
→ A transistor is biased either with the help of battery or associating a circuit with the transistor.
→ The circuit used with the transistor is known as biasing circuit.
→ The proper flow of zero signal collector current (proper operating point of a transistor) and

the maintenance of proper collector-emitter voltage during the passage of signal is known as transistor biasing.

Stabilisation :-

→ The process of making operating point independent of temperature changes or variations in transistor parameter is known as stabilisation.

Or The maintenance of the operating point stable is known as stabilisation.



→ Stabilization of the operating point depends on

a) Temperature dependence of I_C.

b) Individual Variation. (β and V_{BE})

c) Thermal runaway.

→ Thermal runaway depends upon the construction of a transistor

→ The collector junction temp. range lies between 60°C to 100°C for Ge transistor and 150°C to 225°C for Si transistor.

→ If the temperature increases beyond this range then the transistor burns out.

→ The self-destruction of an unstabilized transistor is known as thermal runaway.

Stability factor :- (S)

→ The stability factor (S) is defined as the rate of change of collector current (I_C) w.r.t the reverse saturation current (I_{CO} - collector leakage current), keeping β and V_{BE} constant.

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{\Delta I_C}{\Delta I_{CO}}$$

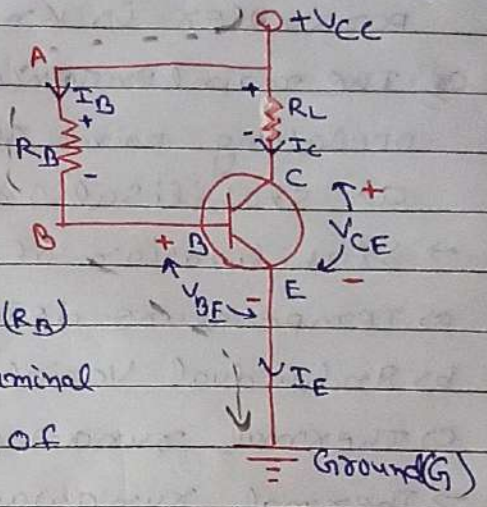
→ Note :- The smaller is the value of S, higher is the stability. So the stability factor (S) should be kept as small as possible.

Different Methods for transistor Biasing :-

→ Some of the methods used for providing bias for a transistor are a) Base resistor Method b) collector to base bias c) voltage divider bias

→ To simple the calculation, we used only one source of supply (V_{CC}) instead of two source of supply (V_{BB} & V_{CC})

Base Resistor Method



→ This figure shows an NPN transistor connected in common-emitter (CE) configuration with resistor biased.

→ In this method, a high resistance (R_B) is connected between positive terminal of supply voltage (V_{CC}) and base of the transistor.

→ Here, the required zero signal base current flows through R_B and is provided by V_{CC}.

→ The base-Emitter junction is forward biased because the base is positive w.r.t emitter.

→ The required value of zero signal base current I_B ($I_C = \beta I_B$) can be made to flow by selecting the proper value of base resistor (R_B).

Circuit analysis :-

→ By applying KVL (Kirchhoff's voltage law) in closed circuit ABEGA, we have got

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow I_B R_B = V_{CC} - V_{BE}$$

$$\Rightarrow \boxed{R_B = \frac{V_{CC} - V_{BE}}{I_B}} \quad -(1)$$

Further $\beta = \frac{I_C}{I_B} \Rightarrow \boxed{I_B = \frac{I_C}{\beta}} \quad -(2)$ β = Base current amplification factor

Put the value of Eqn (2) in Eqn (1)

$$R_B = \frac{V_{CC} - V_{BE}}{I_C/\beta} \Rightarrow \boxed{R_B = \frac{(V_{CC} - V_{BE})\beta}{I_C}} \quad -(3)$$

Since V_{BE} is generally very small as compared to V_{cc}, hence $\boxed{R_B = \frac{\beta V_{cc}}{I_C}}$ —(4)

→ The whole method is also called as fixed-bias method.

Q/ A germanium transistor is to be operated at zero signal $I_C = 1mA$. If the collector supply $V_{cc} = 10V$, what is the value of R_B in base resistor method? ($\beta = 100$).

Ans:- $R_B = \frac{(V_{cc} - V_{BE})\beta}{I_C}$ for Germanium (V_{BE}) = 0.3V

$V_{cc} = 10V$, $\beta = 100$

$I_C = 1mA = 1 \times 10^{-3} A$.

$= \frac{(10 - 0.3)100}{1 \times 10^{-3}} = 970000\Omega$ or $970K\Omega$ (Ans)

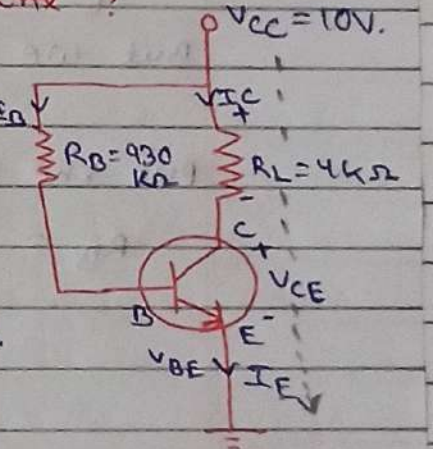
Q/ A silicon transistor with $\beta = 100$, $V_{cc} = 10V$, $R_B = 930K\Omega$ & $R_L = 4K\Omega$. Determine the operating point (V_{CE}, I_C)?

Ans:- Given $V_{cc} = 10V$, $\beta = 100$, $R_B = 930K\Omega$

$R_L = 4K\Omega = 4 \times 10^3 \Omega$, $V_{BE} = 0.7V$ (Silicon)

then $I_C = \frac{(V_{cc} - V_{BE})\beta}{R_B}$

$= \frac{(10 - 0.7) \times 100}{930 \times 10^3} = 1mA$ or $1 \times 10^{-3} A$.



Now apply KVL on outside loop,

$V_{cc} - I_C R_L - V_{CE} = 0$

$\Rightarrow V_{CE} = V_{cc} - I_C R_L \Rightarrow V_{CE} = 10 - 1 \times 10^{-3} \times 4 \times 10^3 = 6V$.

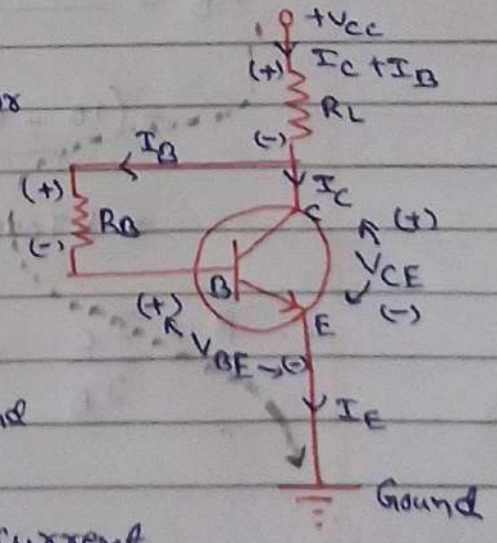
∴ Operating point $(V_{CE}, I_C) = (6V, 1mA)$ (Ans)

Collector to Base Bias

→ This figure shows an NPN transistor connected in common-emitter (CE) configuration with collector to base bias.

→ In this method, one end of (R_B) is connected to the base & the other end to the collector.

→ Here, the required zero signal base current



is determind not by V_{CC} but by the collector-base voltage (V_{CB})

→ Since V_{CB} is forward bias, hence I_B flows through R_B. This causes the zero signal collector current to flow in the circuit.

Circuit analysis :-

→ For finding R_B :-

voltage drop across $(R_L) V_L = (I_C + I_B) R_L \cong I_C R_L$

(∵ Since I_B has very small value)

* By Applying KVL, inside the circuit :-

$$V_{CC} - I_C R_L - I_B R_B - V_{BE} = 0$$

$$\Rightarrow I_B R_B = V_{CC} - V_{BE} - I_C R_L$$

$$\Rightarrow \boxed{R_B = \frac{V_{CC} - V_{BE} - I_C R_L}{I_B}} \quad -(1)$$

But we know $\beta = \frac{I_C}{I_B} \Rightarrow \boxed{I_B = \frac{I_C}{\beta}} \quad -(2)$

Put the value of Eqn (2) in Eqn (1)

$$R_B = \frac{V_{CC} - V_{BE} - I_C R_L}{I_C/\beta} \Rightarrow \boxed{R_B = \frac{(V_{CC} - V_{BE} - I_C R_L)\beta}{I_C}} \quad -(3)$$

or $$\boxed{I_C = \frac{(V_{CC} - V_{BE} - I_C R_L)\beta}{R_B}}$$

Q/ In a collector to Bias circuit $I_C = 1mA$, $V_{CE} = 5V$, $\beta = 100$, $R_L = 4k\Omega$, $V_{CC} = 10V$, $V_{BE} = 0.3V$, Find R_B, I_B & operating point (V_{CE}, I_C) ?

Ans :-

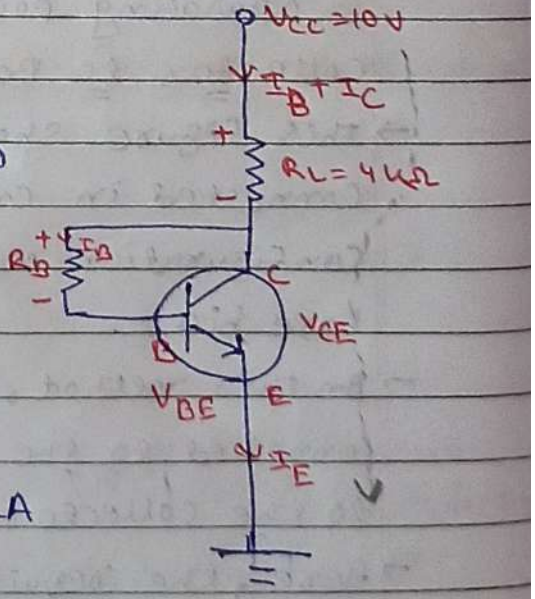
$$R_B = \frac{(V_{CC} - V_{BE} - I_C R_L)\beta}{I_C}$$

$$= \frac{(10 - 0.3 - 1\times10^{-3} \times 4\times10^{3})100}{1\times10^{-3}}$$

$$= 570000\Omega \text{ or } 570k\Omega$$

$$\therefore \beta = \frac{I_C}{I_B} \Rightarrow I_B = \frac{I_C}{\beta} = \frac{1\times10^{-3}}{100}$$

$$= 1\times10^{-5} = 10\mu A$$



Applying KVL,

$V_{CC} - (I_B + I_C)R_L - V_{CE} = 0$ (since the value of I_B is very small so we neglected I_B)

$\Rightarrow V_{CE} = V_{CC} - I_C R_L$

$\Rightarrow V_{CE} = 10 - 1\times10^{-3} \times 4\times10^{3} = 6\,V.$

$\therefore$ operating point $(V_{CE}, I_C) = (6V, 1mA)$ (Ans)

Self Bias or Emitter Bias (Voltage Divider Bias)

→ This is the most widely used method of providing biasing and stabilization to a transistor.

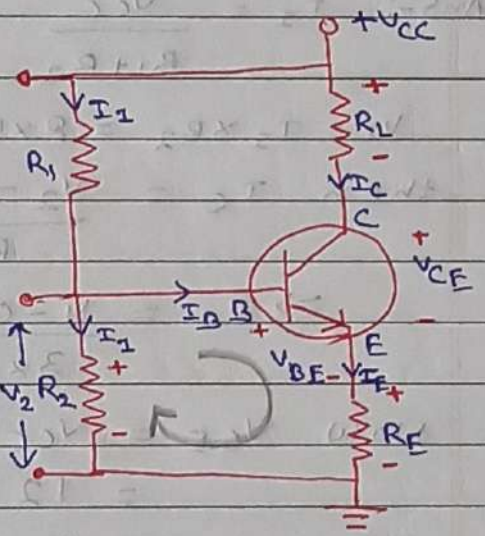
→ This is also known as universal bias stabilization circuit.

→ In this method, two resistance R_1 and R_2 are connected across the supply voltage V_{CC} and provide biasing.

→ The emitter resistance (R_E) provides stabilization.

→ The name "Voltage divider" comes from the voltage divide formed by R_1 and R_2.

→ The voltage drop across R_2 is forward biases for the base-emitter junction.



Circuit analysis :-

→ Let current I_1 flows through R_1.

→ As the base current (I_B) is very small, the current flowing through R_2 can also be taken as I_1.

→ The calculation of collector current (I_C) is as follows:-

$$I_1 = \frac{V_{CC}}{R_1 + R_2} \quad \text{---(1)}$$

→ The voltage (V_2) developed across R_2 is given by

$$V_2 = I_1 R_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2 \quad -(2)$$

→ Applying KVL to the base circuit, we have

$I_1 R_2 - V_{BE} - I_E R_E = 0$ $(\because V_2 = I_1 R_2)$

$\Rightarrow V_2 - V_{BE} - I_E R_E = 0$

$\Rightarrow V_2 - V_{BE} - I_C R_E = 0$ ($\because I_E = I_B + I_C$ But I_B is very small, so neglected) therefore $I_E \simeq I_C$)

$\Rightarrow I_C R_E = V_2 - V_{BE}$

$\Rightarrow \boxed{I_C = \frac{V_2 - V_{BE}}{R_E}}$ — (3)

→ Now, for the collector emitter voltage (V_{CE}) can be calculated as follows -:

* By Applying KVL to the collector Side, we have

$V_{CC} - I_C R_L - V_{CE} - I_E R_E = 0$

$\Rightarrow V_{CC} - I_C R_L - V_{CE} - I_C R_E = 0$ $\because I_E \simeq I_C$

$\Rightarrow V_{CE} = V_{CC} - I_C R_L - I_C R_E$

$\Rightarrow \boxed{V_{CE} = V_{CC} - I_C (R_L + R_E)}$ — (4)

Q/ A silicon transistor uses potential divider method of biasing. $V_{CC} = 12V$, $R_1 = 10K\Omega$, $R_2 = 5K\Omega$, $R_L = 1K\Omega$ and $R_E = 3K\Omega$. Find the operating point. (V_{CE}, I_C)

Ans -: $I_1 = \frac{V_{CC}}{R_1 + R_2} = \frac{12}{(10+5)\times 10^3} = 8 \times 10^{-4} = 0.8 mA$

$V_2 = I_1 \times R_2 = 8 \times 10^{-4} \times 5 \times 10^3 = 4V.$

then $I_C = \frac{V_2 - V_{BE}}{R_E}$ (for silicon $V_{BE} = 0.7V.$)

$\Rightarrow I_C = \frac{4 - 0.7}{3 \times 10^3} = 1.1 \times 10^{-3} = 1.1 mA.$

Now $V_{CE} = V_{CC} - I_C (R_L + R_E)$

$= 12 - 1.1 \times 10^{-3} (1 \times 10^3 + 3 \times 10^3)$

$= 12 - 1.1 \times 10^{-3} \times 10^3 (1 + 3)$

$= 12 - 4.4 = 7.6 V.$

∴ So the operating point (Q) = $(V_{CE}, I_C) = (7.6V, 1.1mA)$ (Ans)

6TH CHAPTER

TRANSISTOR AMPLIFIER AND OSCILLATOR

Single Stage Transistor Amplifier :-

⇒ When only one transistor with associated circuitry is used for amplifying a weak signal, the circuit is known as single stage transistor amplifier.

Practical Circuit of Transistor Amplifier :-

i) **Biasing Circuit** :- The resistance R_1, R_2 and R_E form the biasing and stabilisation circuit. The biasing circuit must establish a Proper operating point.

ii) **Input Capacitor (C_{in})** → An electrolytic capacitor Cin is used to couple the signal to the base of the transistor. The capacitor Cin allows only A.C Sig to flow but isolates the signal source from R_2.

iii) **Emitter by pass Capacitor (C_E)** :- An emitter by pass Capacitor is used in parallel with R_E to provide a low reactance path to the amplified a.c signal.

⇒ If it is not used, then amplified a.c signal flowing through R_E will cause a voltage drop across it, thereby reducing the o/p voltage.

iv) **Coupling Capacitor (C_c)** :-

→ The coupling capacitor couples one stage of amplification to the next stage.

⇒ Cc isolates the d.c of one stage from the next stage, but allows the passage of a.c signal

Circuit Current :-

i Base Current :- when no signal is applied in the ba
Circuit, d.c base current I_B flows due to biasi
circuit. when a.c signal is applied, a.c base current
i_b also flows. i.e

$$i_B = I_B + i_b$$

ii Collector Current :- when no signal is applied, a
d.c collector current I_c flows due to biasing
circuit. when a.c signal is applied a.c collector
current i_c also flows.

$$i_C = I_c + i_c$$

iii Emitter Current :- when no signal is applied, a d.c
emitter current I_E flows. with the application
of signal i_E is given by

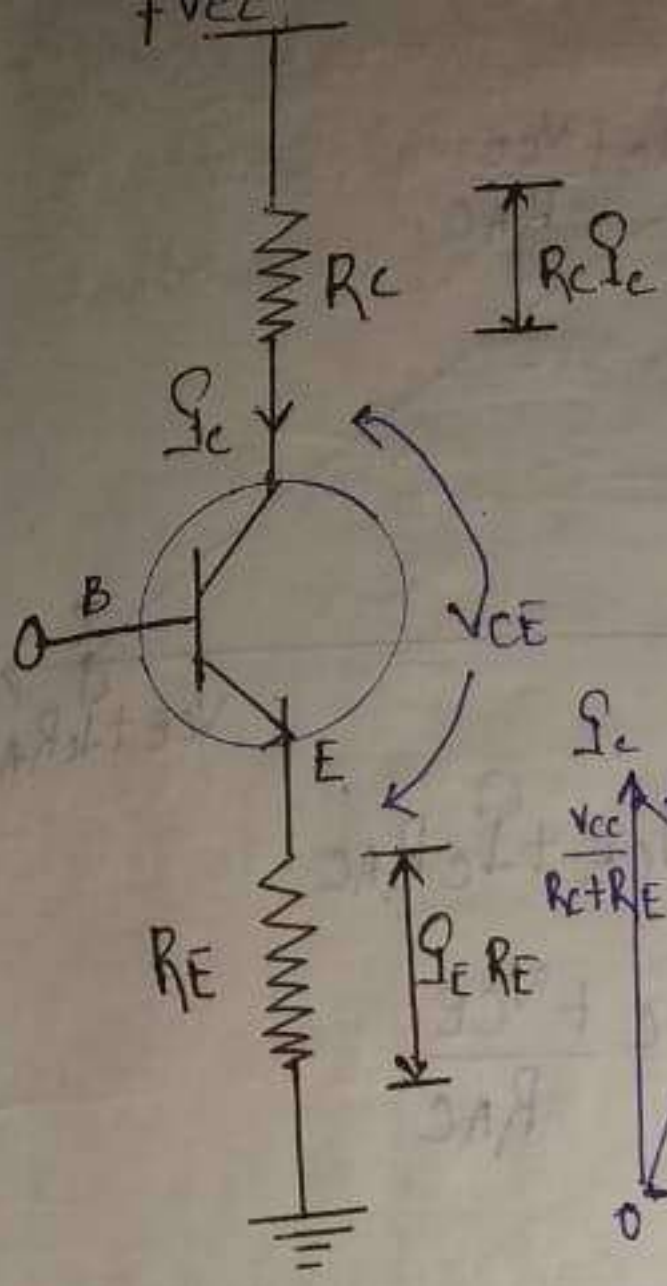
$$i_E = I_E + i_e .$$

Load Line Analysis :-

D.C Load Line :- It is the line on the output characte
of a transistor circuit which gives the value of
I_c & V_{CE} corresponding to Zero signal in d.c condition.

D.C Equivalent Circuit :- In the d.c equivalent circui
of transistor amplifier, only d.c condition are
Consider. So d.c current can not flow through the
Capacitor, So the following two steps are applied.

a) Reduce all sources to Zero



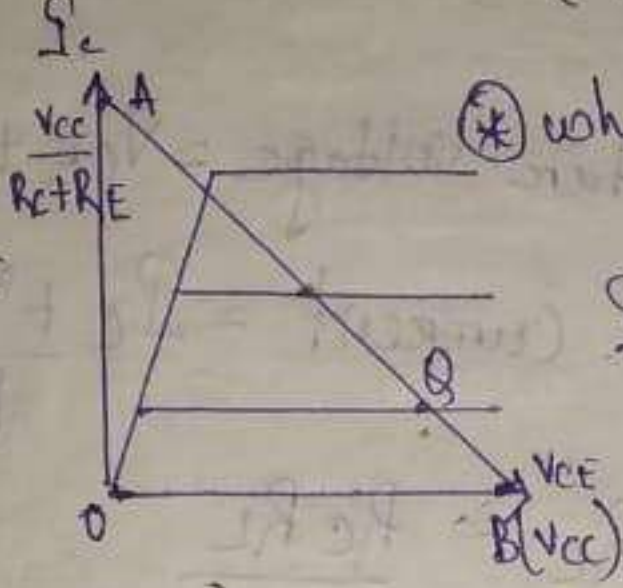
Applying KVL,

$V_{CC} = R_C I_C + V_{CE} + R_E I_E = 0$

$\Rightarrow V_{CE} = V_{CC} - I_C R_C - I_E R_E$

$\Rightarrow V_{CE} = V_{CC} - I_C(R_C + R_E)$

$(\because I_E \simeq I_C)$



(*) when V_{CE} will Max^M, when $I_C = 0$
i.e $V_{CE} = V_{CC}$
It locates the 'B' point on graph.

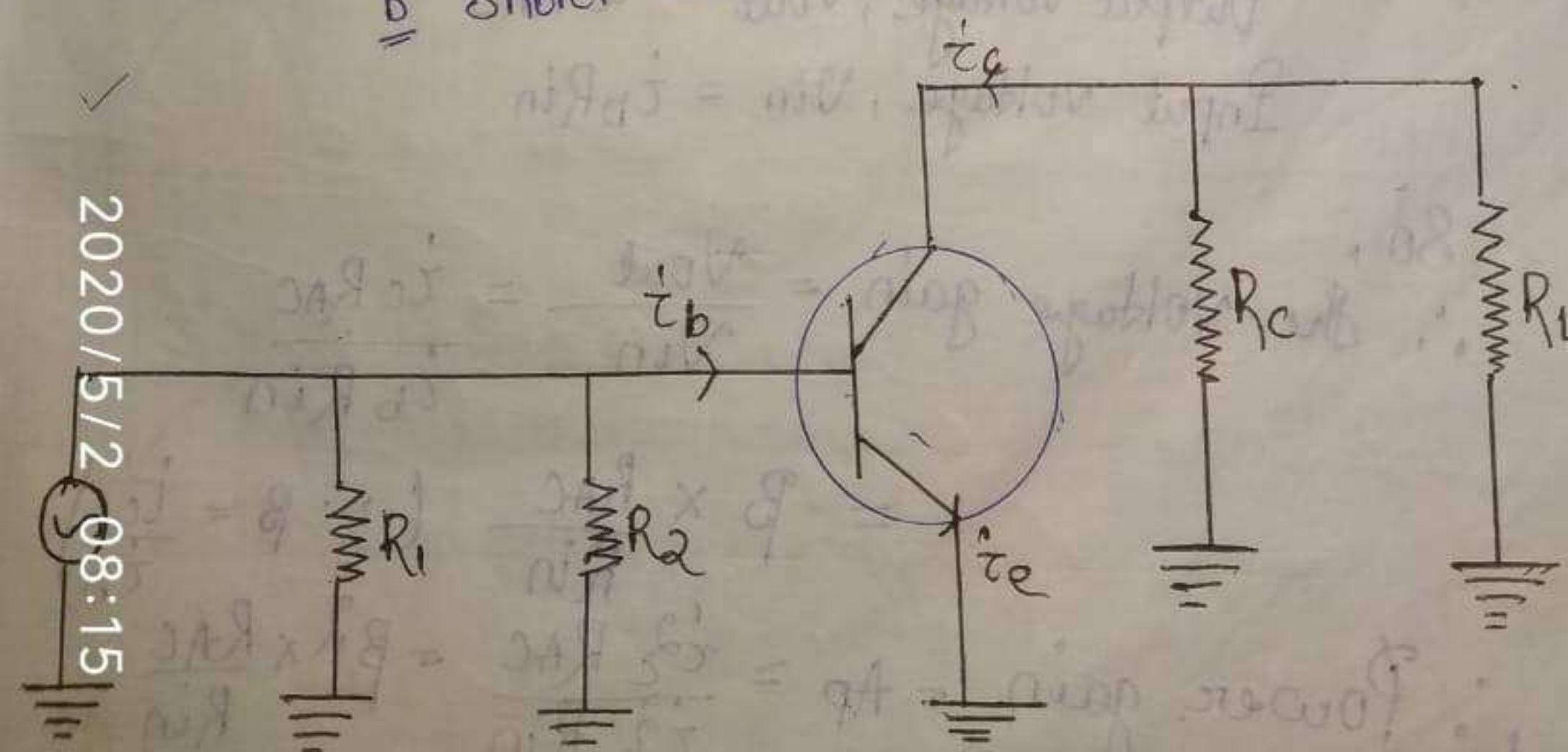
A·C Load Line :- This is the line on the o/p characteristic of a transistor circuit which gives the values of I_C & V_{CE} when the signal is applied.

A·C Equivalent Circuit → The capacitors are generally used to couple or bypass the a·C signal.

Following two steps are Consider

a Reduce all sources to Zero

b Short all the capacitor

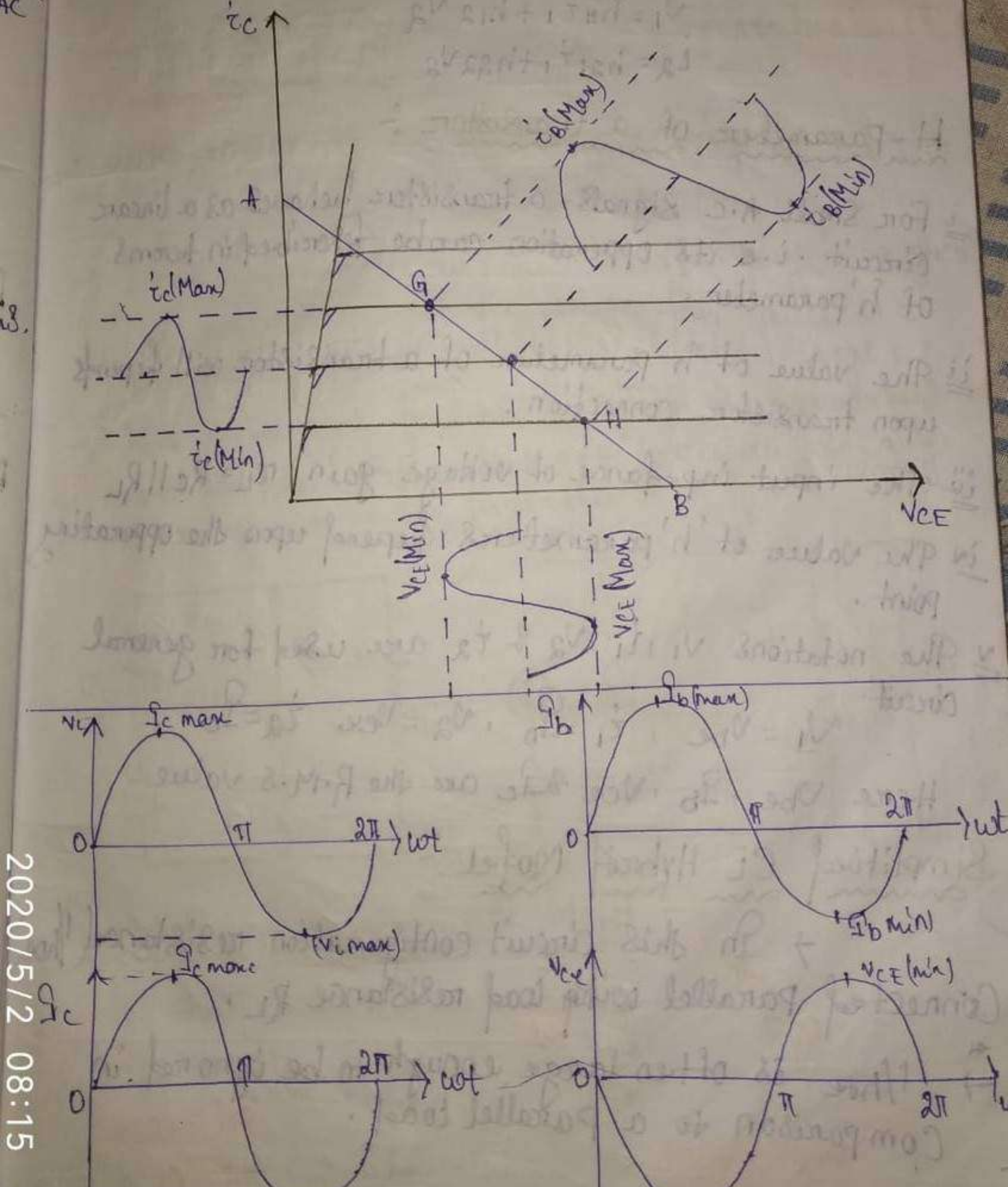


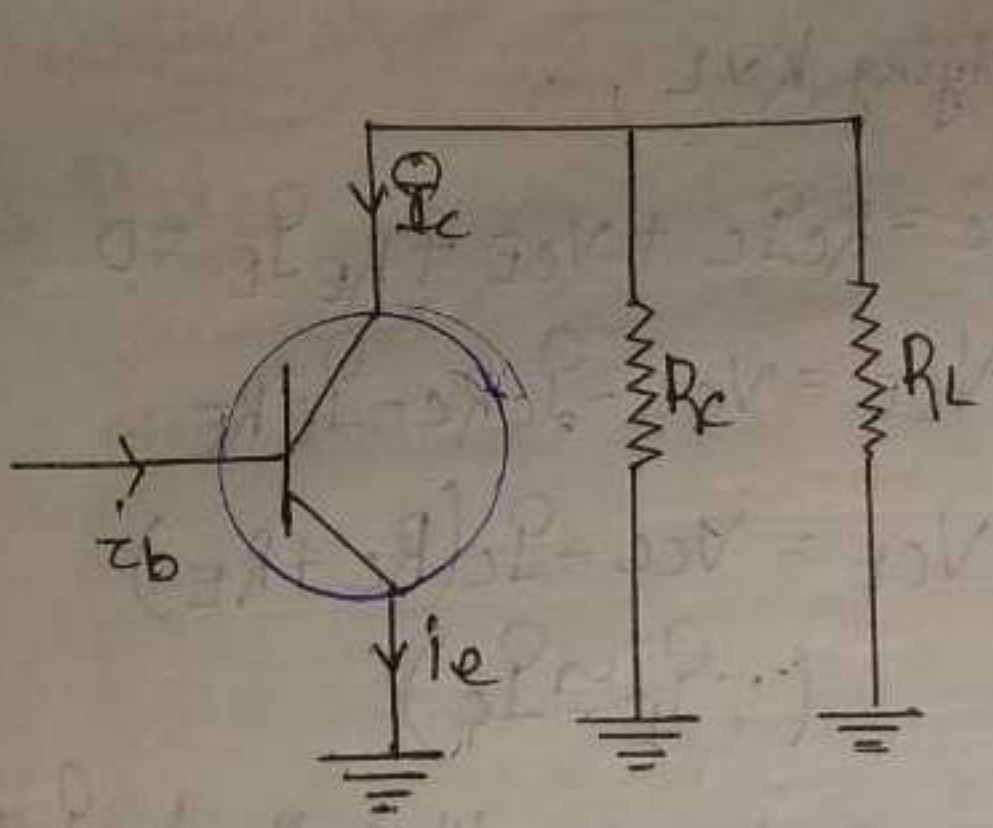
Phase Reversal :- The phase difference of 180° between the signal voltage and output voltage in a common emitter amplifier is known as phase reversal.

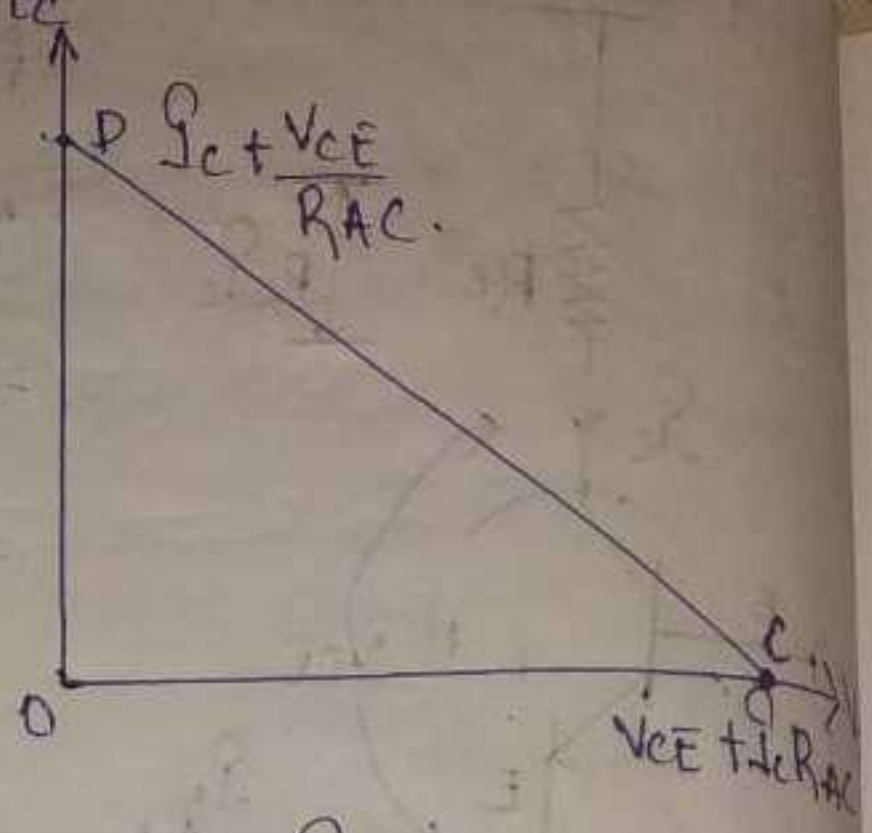
$$V_{CE} = V_{CC} - i_c R_c \quad \text{---(i)}$$

$$V_{CE} = 0 - i_c R_c$$

$$V_{CE} = -i_c R_c$$







Max. Collector Emitter voltage = $V_{CE} + I_C R_{AC}$

Max^m collector current = $I_C + \frac{V_{CE}}{R_{AC}}$

$$R_{AC} = R_C \parallel R_L = \frac{R_C R_L}{R_C + R_L}$$

∴ 'D' points locates a.c load line on the collector axis

Voltage Gain / Calculation of Gain :-

It is the ratio of a.c output voltage to the a.c input signal voltage.

$$\text{a.c load } R_{AC} = R_C \parallel R_L = \frac{R_C \times R_L}{R_C + R_L}$$

Output voltage, $V_{out} = i_c R_{AC}$

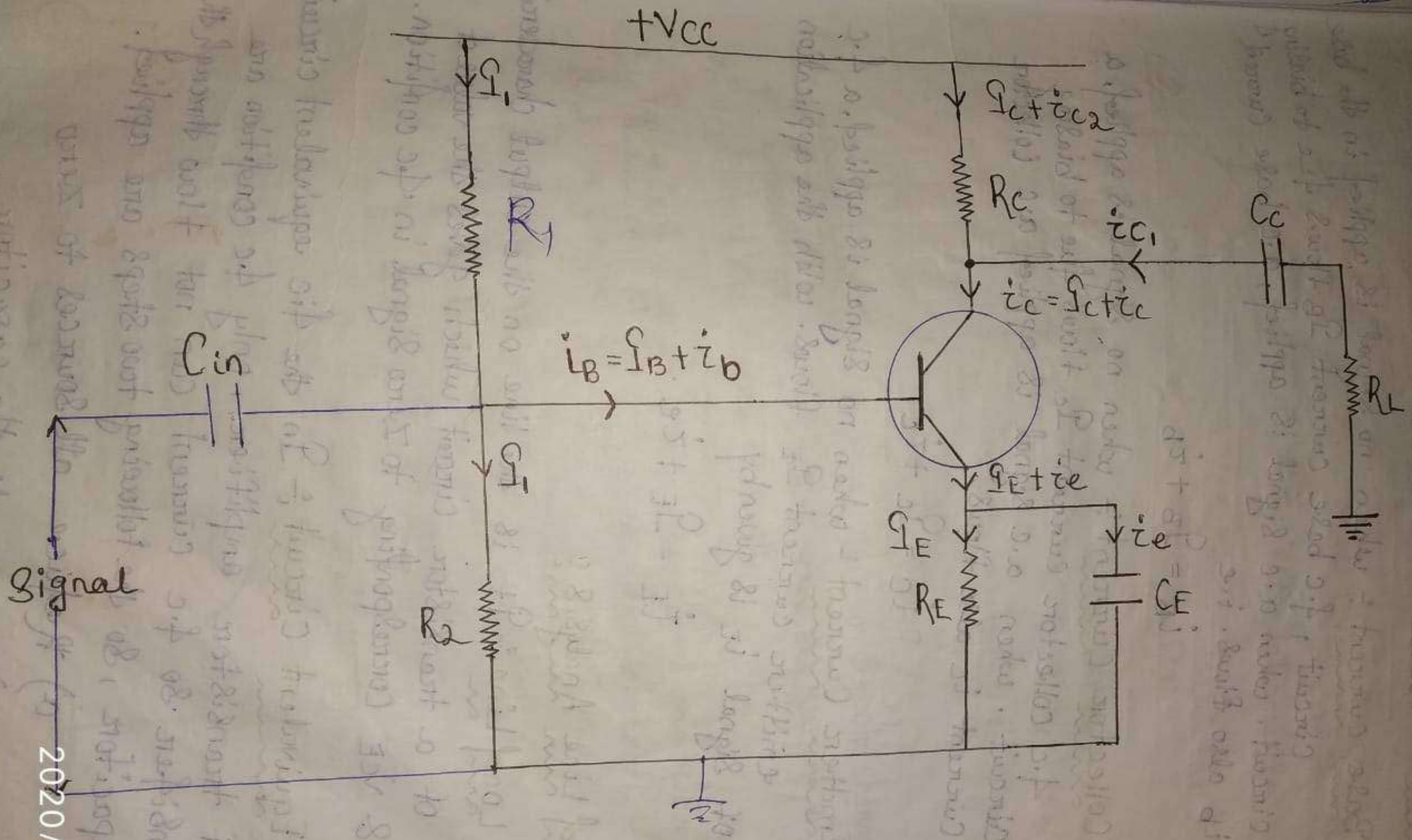
Input voltage, $V_{in} = i_b R_{in}$

So,

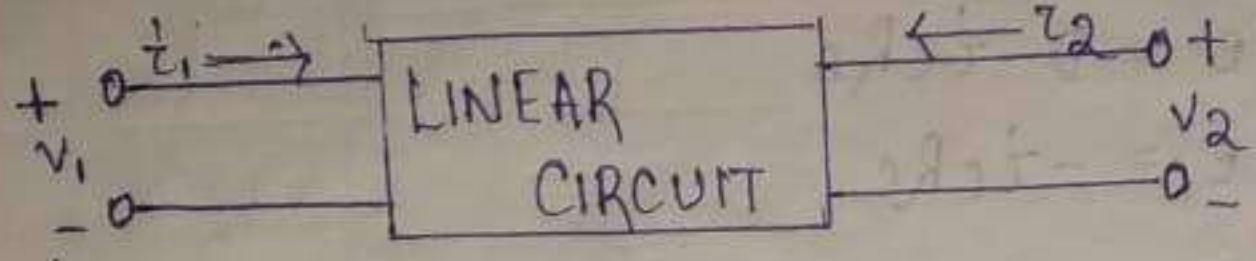
∴ the voltage gain $= \frac{V_{out}}{V_{in}} = \frac{i_c R_{AC}}{i_b R_{in}}$

$= \beta \times \frac{R_{AC}}{R_{in}}$ $\left(\because \beta = \frac{i_c}{i_b}\right)$

∴ Power gain $= A_P = \frac{i_c^2 R_{AC}}{i_b^2 R_{in}} = \beta^2 \times \frac{R_{AC}}{R_{in}}$


+Vcc
I_1
R_1
$I_C + i_{c2}$
R_C
i_{c1}
C_C
$i_C = I_C + i_c$
C_{in}
$i_B = I_B + i_b$
R_L
I_1
$I_E + i_e$
Signal
I_E
i_e
R_2
R_E
C_E

Hybrid Parameter → Every linear circuit having input and output terminal can be analysed by four parameters (one measured in ohm, one in mho & two dimensionless) called hybrid parameter.



$$v_1 = h_{11} i_1 + h_{12} v_2$$
$$i_2 = h_{21} i_1 + h_{22} v_2$$

H-Parameter of a transistor :-

i) For small A.C signals, a transistor behaves as a linear circuit. i.e. its opperation can be described in terms of 'h' parameter.

ii) The value of h parameter of a transistor will depend upon transistor connection.

iii) The input impedance of voltage gain. $r_L = R_C \| R_L$

iv) The value of 'h' parameters depend upon the opperating point.

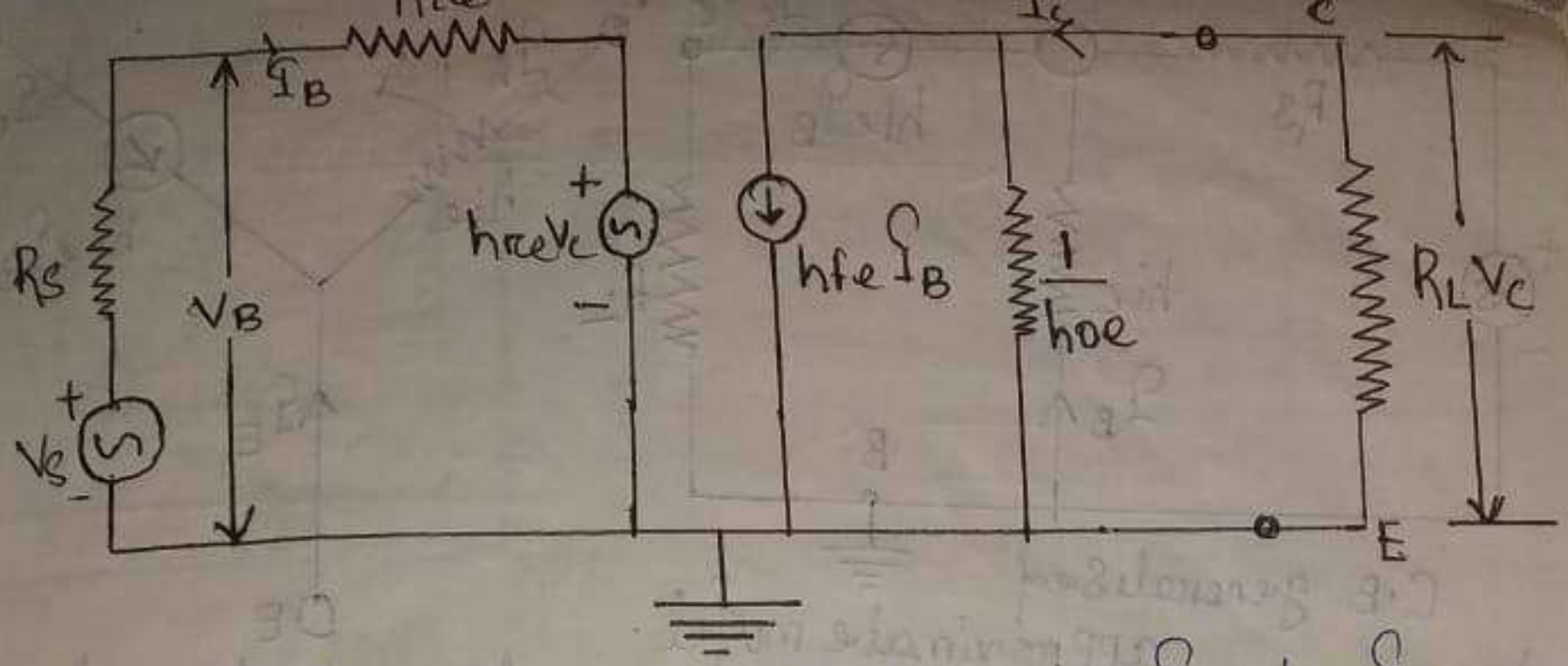
v) The notations v_1, i_1, v_2 & i_2 are used for general circuit. $v_1 = v_{be}$, $i_1 = I_b$, $v_2 = v_{ce}$ $i_2 = I_c$.

Here v_{be}, I_b, v_{ce} & I_c are the R.M.S value.

Simplified CE Hybrid Model :-

→ In this circuit configuration resistance connected parallel with load resistance R_L.

→ $1/h_{oe}$ is often large enough to be ignored in comparison to a parallel load.



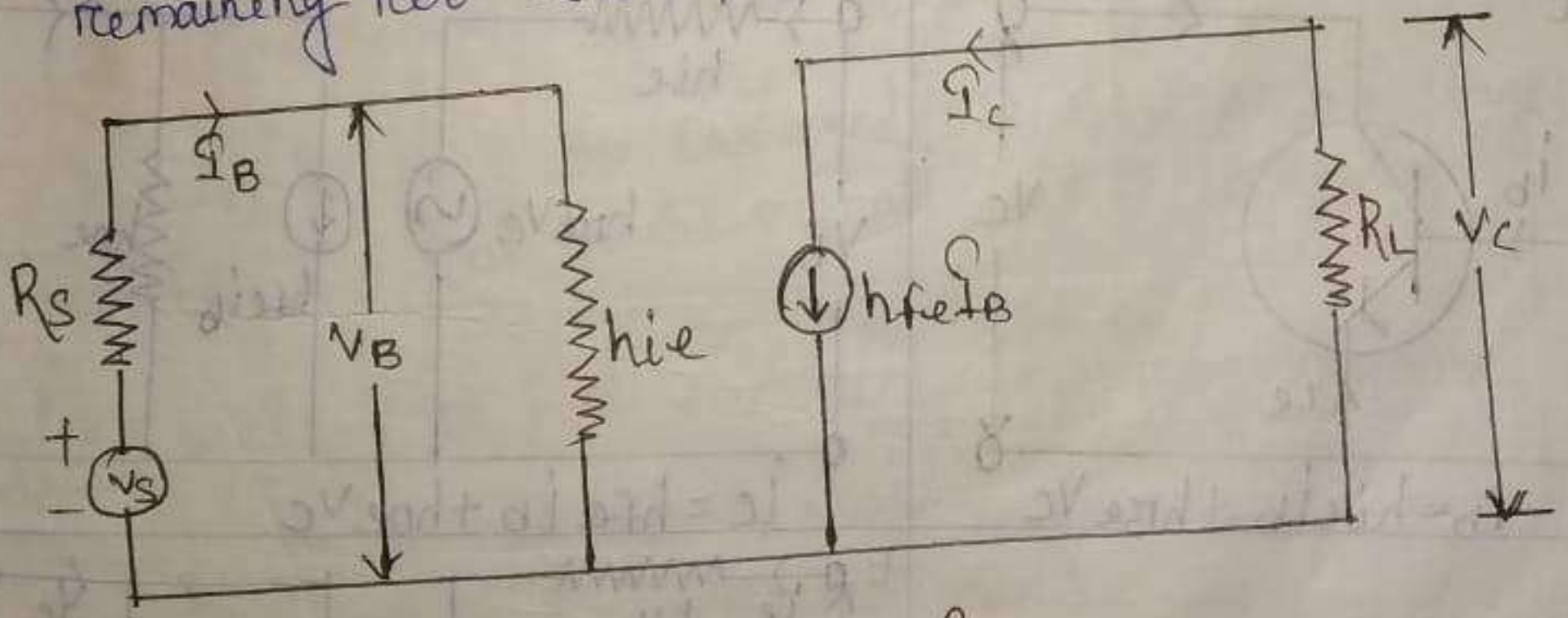
→ The collector current is given by $I_C = h_{fe} I_B$.
Further $V_C = I_C R_L = h_{fe} I_B R_L$

→ Magnitude of voltage is given by.

$$h_{re}|V_C| = h_{re}\, h_{fe}\, I_B R_L$$

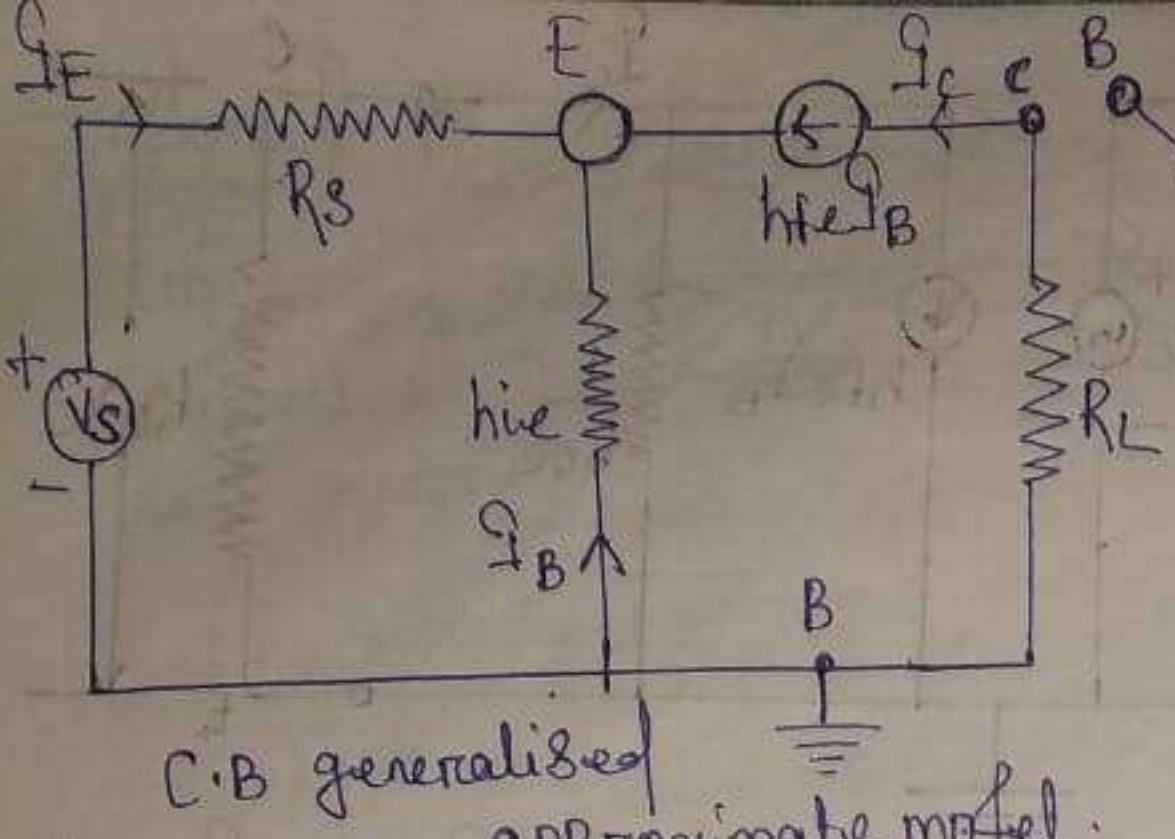
→ Since, $h_{re}\, h_{fe} = 0.01$, this voltage may be neglected in comparison with the voltage drop across $h_{ie} = h_{ie} I_B$ Provided that R_L is not too large.

→ Thus it becomes possible to neglect the parameters and hre in approximate CE h-model. Use only remaining two other parameter.

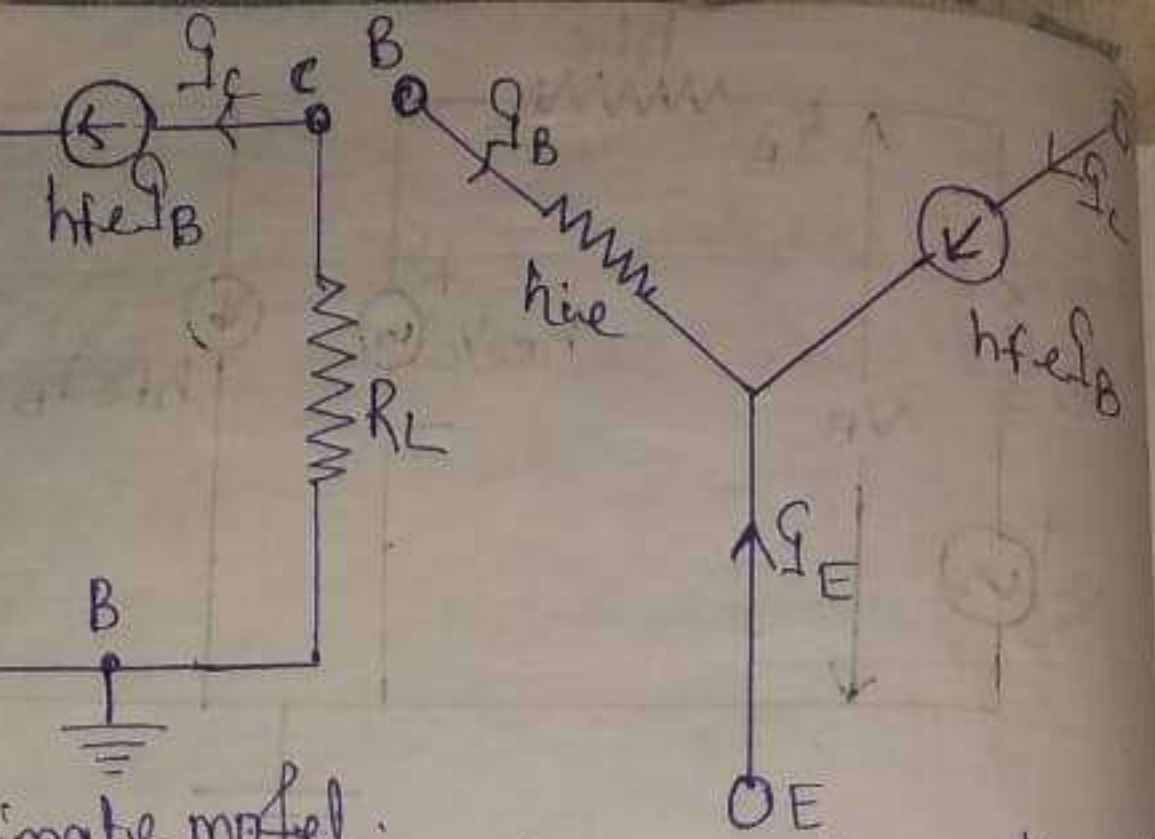


Generalized Approximate Model :-

	CE	CB	CC
$h_{11} = h_i$	h_{ie}	h_{ib}	h_{ic}
$h_{12} = h_r$	h_{re}	h_{rb}	h_{rc}
$h_{21} = h_f$	h_{fe}	h_{fb}	h_{fc}
$h_{22} = h_o$	h_{oe}	h_{ob}	h_{oc}



C.B generalised approximate model.

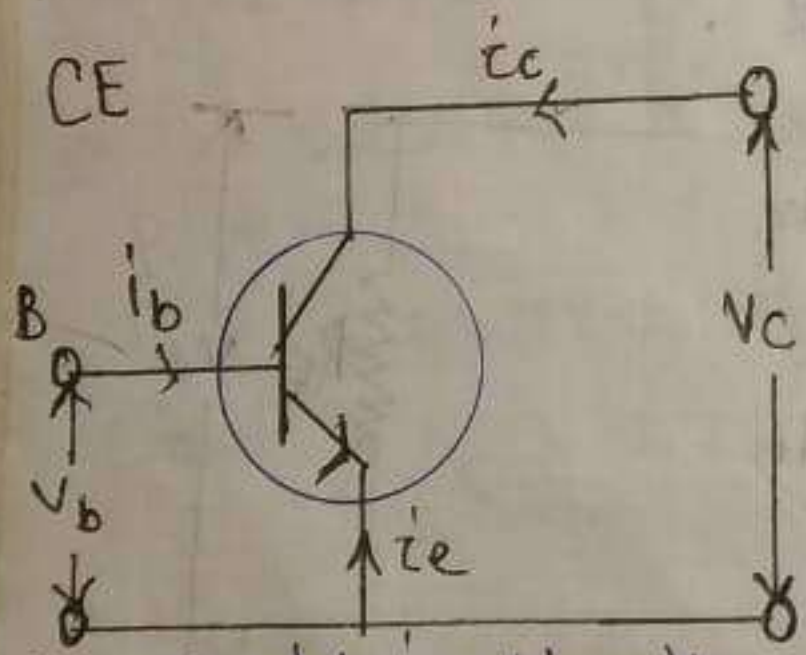
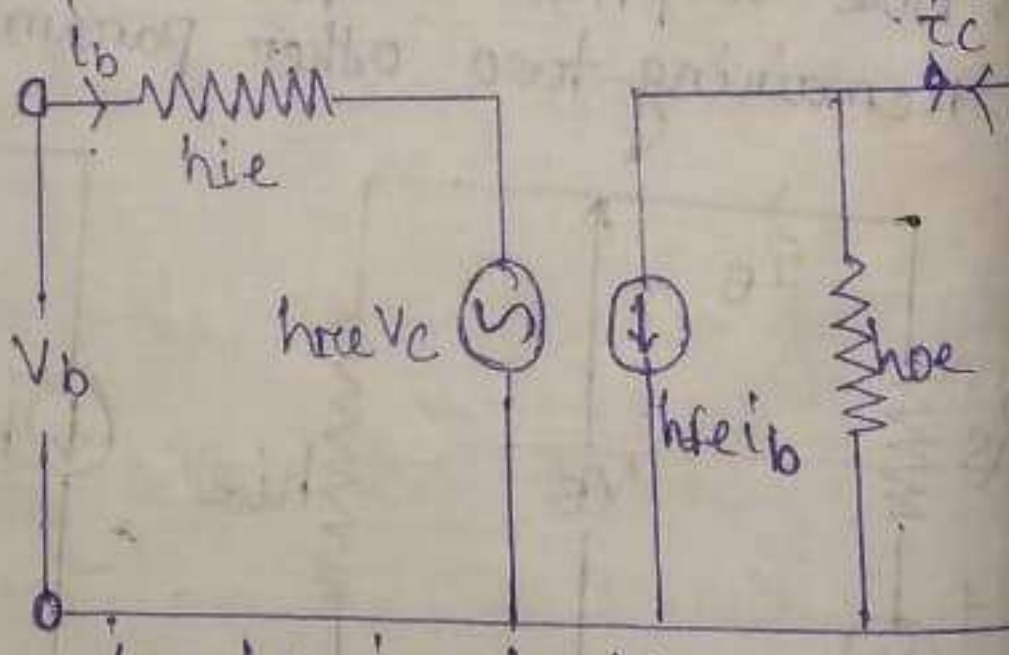
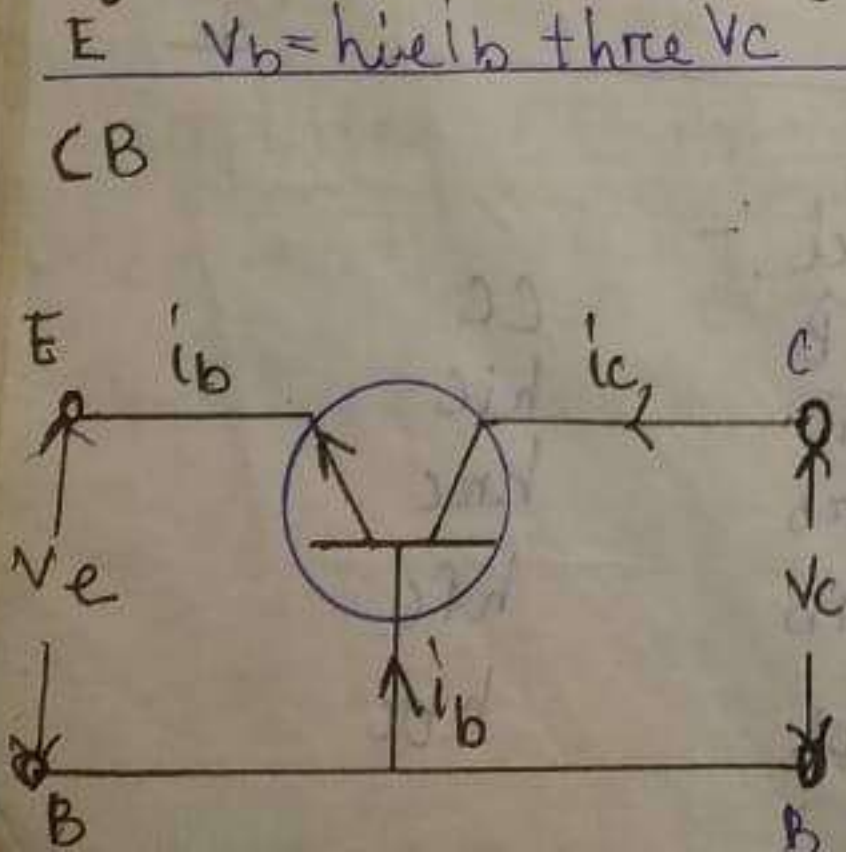
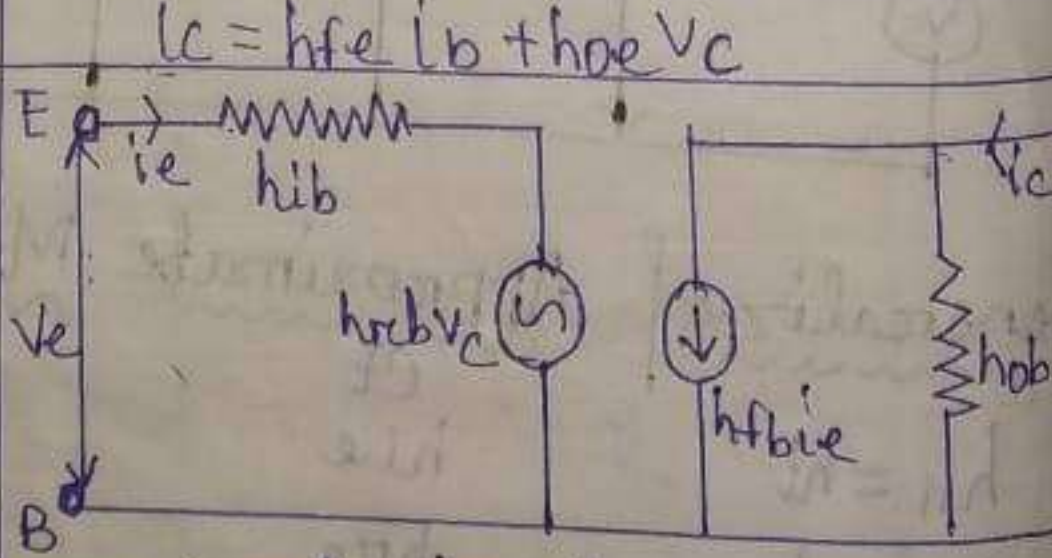


Approximate hybrid model
Valid for all config

→ we first make input & output points E and C along with common terminal B.

→ Now we put current source $h_{fe}I_B$ bet^n E & C & h_{ie} bet^n E and B.

→ The load is connected bet^n collector & base this represents the equivalent circuit of C.B. config

Circuit	Hybrid Model
CE  $V_b = h_{ie}i_b + h_{re}V_c$	 $i_c = h_{fe}i_b + h_{oe}V_c$
CB 	
	$V_e = h_{ib}i_e + h_{rcb}V_c$
	$i_c = h_{fb}i_e + h_{ob}V_c$

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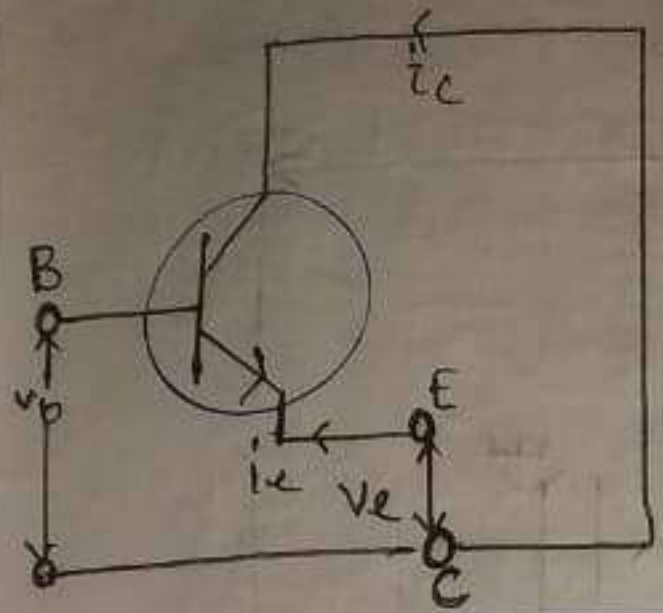
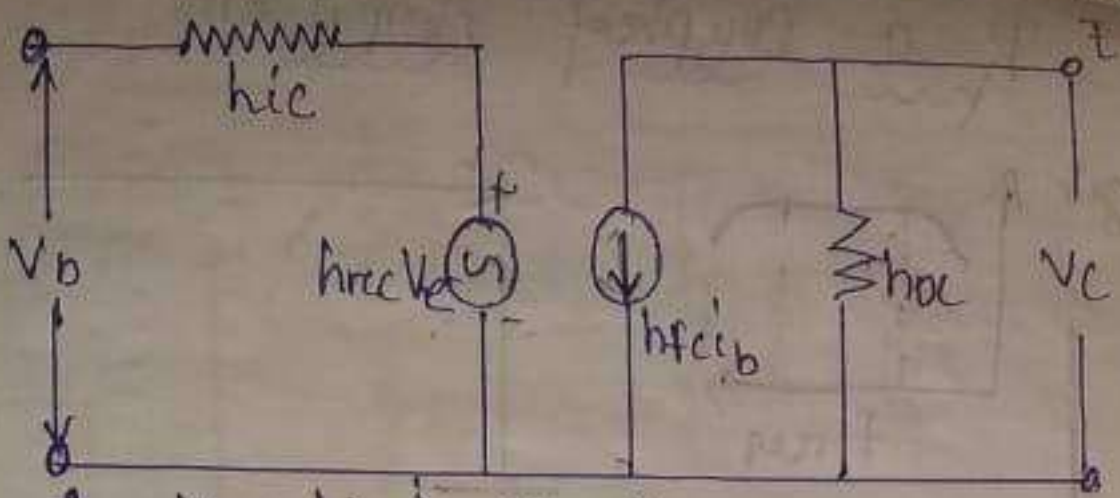




$V_b = h_{ic} i_b + h_{rc} V_e$

$i_e = h_{fc} i_b + h_{oc} V_e$

Multistage Transistor Amplifier

→ A transistor circuit containing more than one stage of amplification is known as multistage transistor amplifier.

R-C Coupled Amplifier :-

→ When a.c signal applied to the base of first transistor, it appears in the amplified from across its Collector load R_C.

→ The amplified ~~load~~ signal developed across R_C is given to base of next stage through the Coupling capacitor (C_C.) The second stage does further amplification of the sig

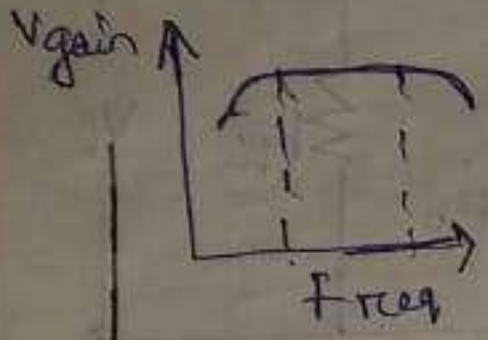
→ In this way, the cascaded (one after another) stages amplify the signal & the overall gain is increased.

Advantages :- i It has excellent frequency response
ii It has lower cost
iii Circuit is very compact.

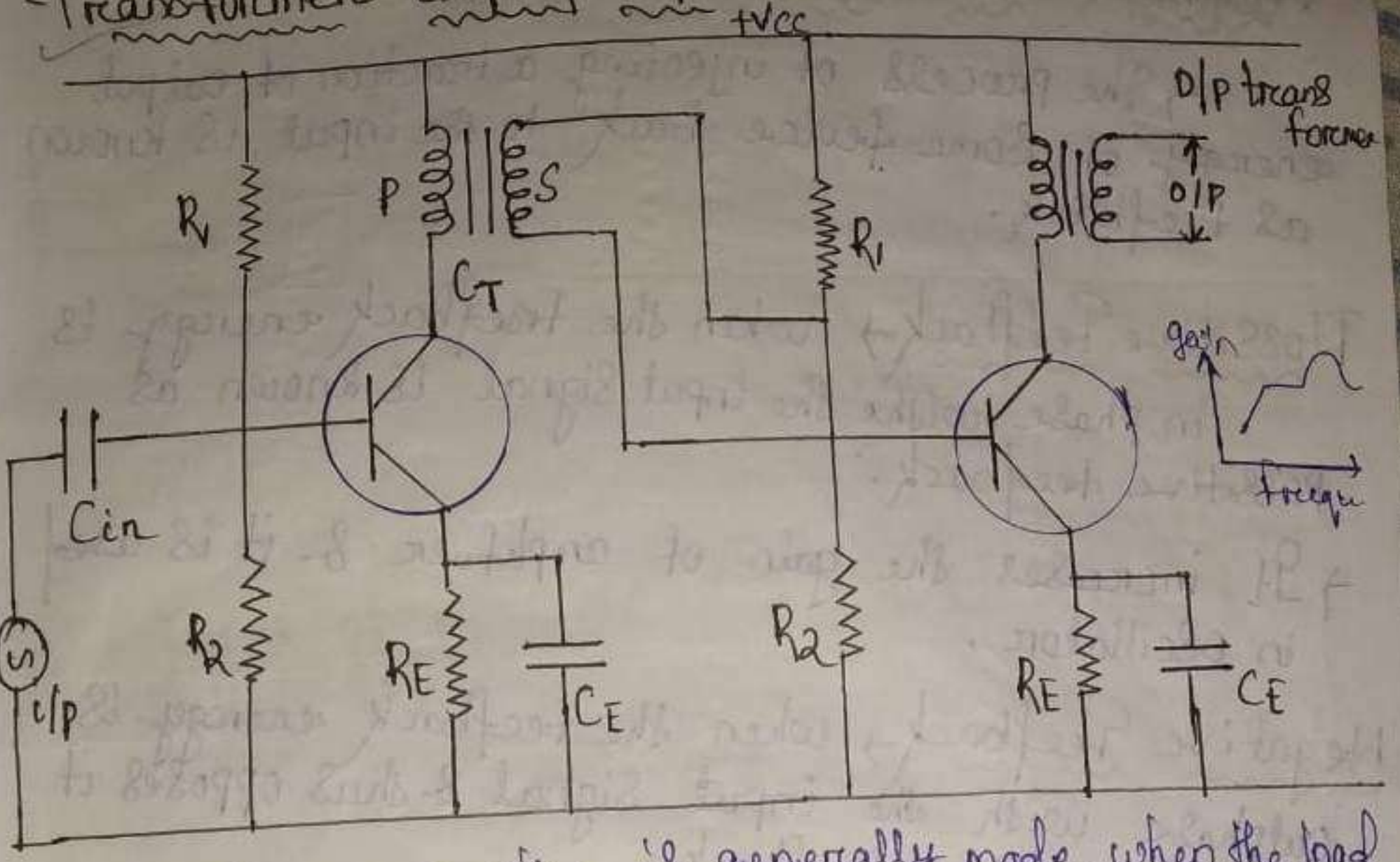
Disadvantages → i Low voltage & power gain.
ii More noisy in moist climates
iii Impedance Matching Poor.

Application → Voltage Amplifier.

R-C Coupled Amplifier



Transformer Coupled Amplifier



→ Transformer coupling is generally made when the load is small. It is mostly used for power amplification.

→ A coupling transformer is used to feed the output of one stage to the input of the next stage.

→ A Primary P of this transformer is made the collector load & its secondary S gives input to the next stage.

→ when a.c signal is applied to the base of first transistor it appears in the amplified from across primary P of the coupling transformer. The voltage developed across primary is transfered to the input of next stage by the secondary.

Advantages → No signal power is lost in the C or B resistor
→ Excellent impedance matching
→ Higher gain

Disadvantages → Poor frequency response
Frequency distortion is high.

Feedback in Amplifier

→ The process of injecting a fraction of output energy of some device back to the input is known as feedback.

Positive Feedback → when the feedback energy is in phase with the input signal is known as positive feedback.

→ It increases the gain of amplifier & it is used in oscillator.

Negative Feedback → when the feedback energy is outphase with the input signal & thus opposes it is called negative feedback.

→ The negative feedback reduces the gain of amplifier.
→ It increases bandwidth, stability in gain.

Negative feedback circuit :-

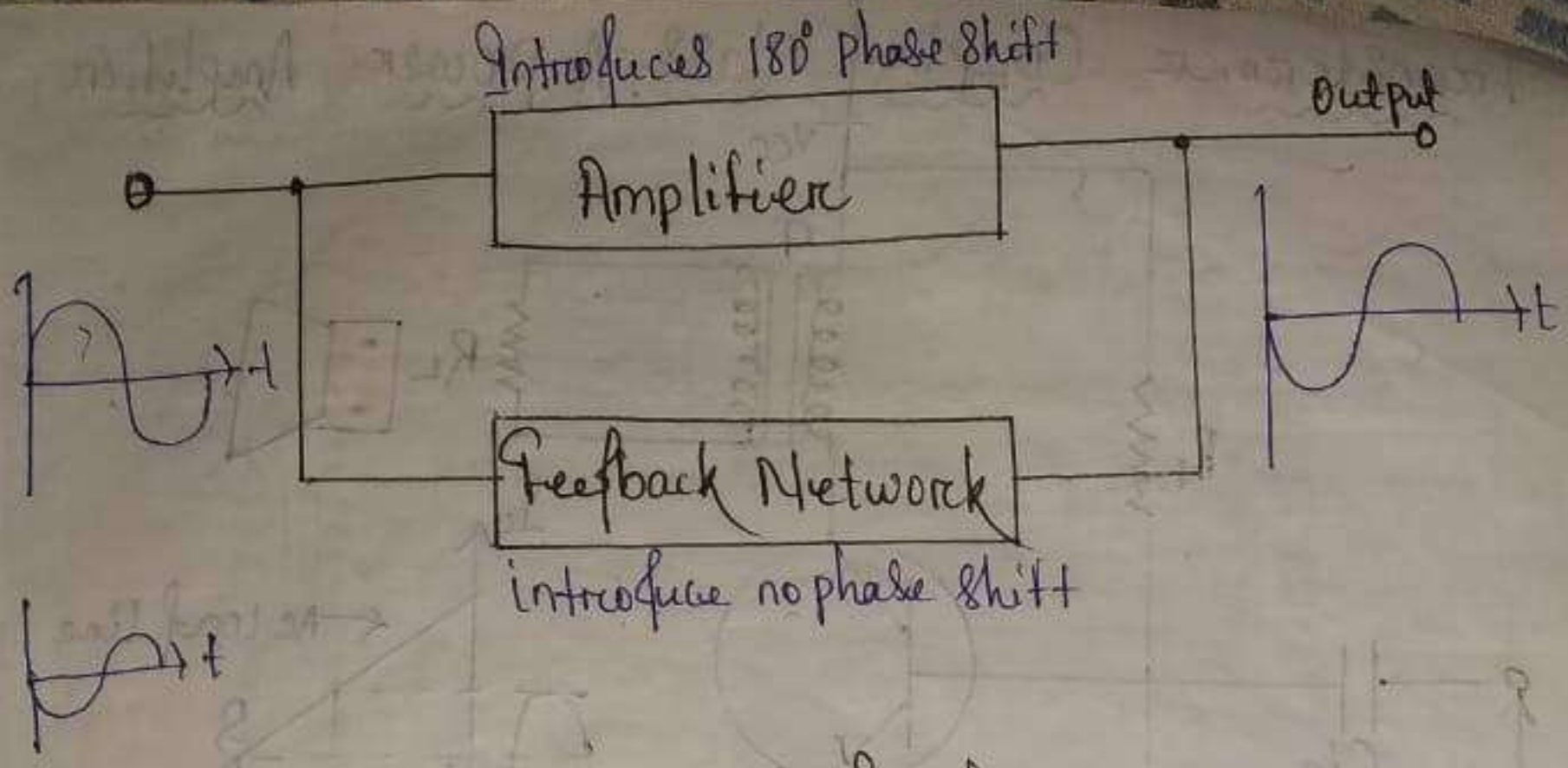
→ when the feedback signal is out of phase with the input signal and thus opposes it the it is called negative feedback circuit.

→ The negative feedback amplifier introduces a phase shift of 180° in the input while the feedback network introduces no phase shift i.e feedback network is designed in such a way it does not introduce any phase shift.

→ There are two types of negative feedback

i Negative voltage feedback

ii Negative Current feedback.



Advantages of Negative feedback :-

i Stabilization of gain / High stability
ii Reduction is distortion (Non-linear distortion of op)
iii Reduction in Noise
iv Change in input impedance / high input
v change in output impedance (1+Aβ times of Z_o)
vi Increase in Bandwidth

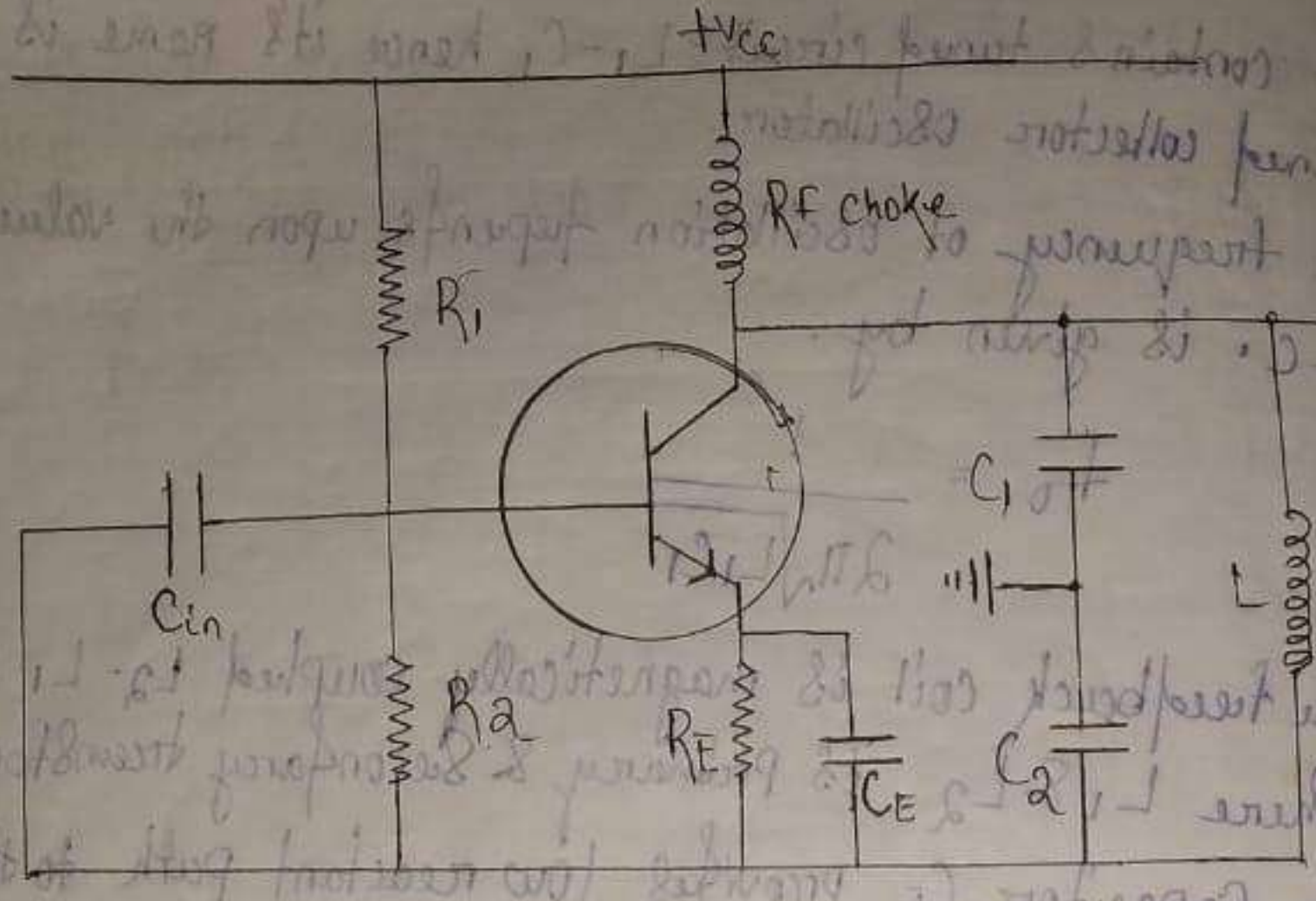
$Z = \sqrt{R^2 - X_C^2}$

$Z = \sqrt{R^2 + (X_L - X_C)^2}$

Power Amplifier & it's classification :-

→ A transistor amplifier which raises the power level of the signal that have audio frequency range is known as transistor audio power amplifier

Voltage Amplifier	Power Amplifier
→ β value is high (>100)	→ β value is low (5 to 20)
→ R_C value high (4-10KΩ)	→ R_C value is low (5 to 20Ω)
→ Coupling - R-C coupling	→ Transformer Coupling
→ Input voltage low (in mv)	→ Input voltage is high (2-4V)
→ Collector Current low	→ Collector Current high
→ power output low	→ power output high
→ Output impedance high	→ Output impedance low.



→ when the circuit is turned on, the capacitors C_1 and C_2 are charged. The capacitor discharge through L.

→ Frequency determine by - The o/p voltage of the amplifier appears across C_1 and feedback voltage is develop across C_2.

→ The voltage across it is 180° out of phase with the voltage drop across C_1 (V_{out}).

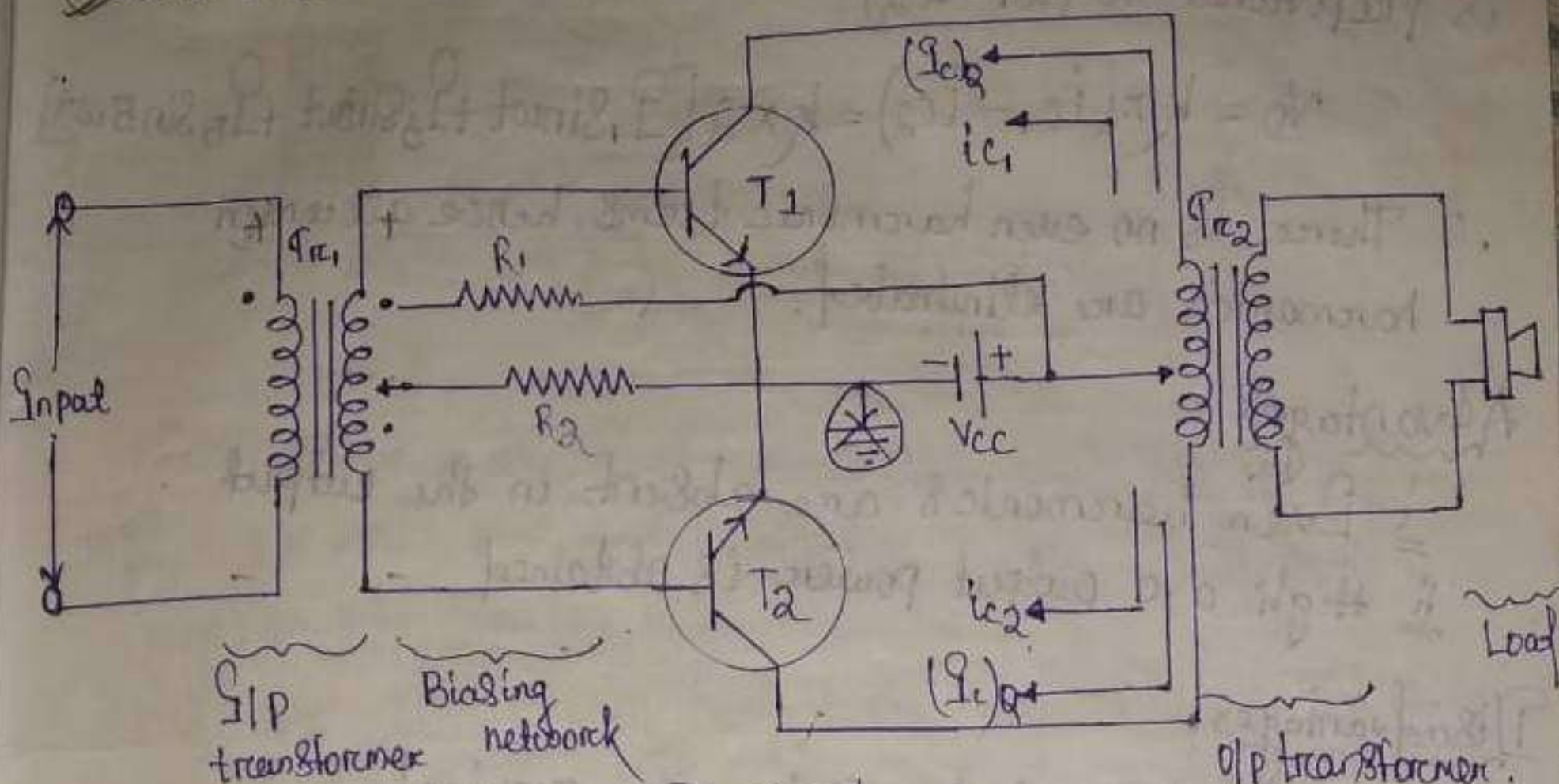
⇒ It is easy to see the voltage feedback to the transistor provides positive feedback.

→ A phase shift 180° is produced by the transistor and a further phase shift of 180° is produced by C_1-C_2 voltage divider.

→ In this way feedback is properly phased to produce continuous undamped oscillation.

$$\therefore A_v = \frac{C_1}{C_2} \quad (\text{Feedback fraction})$$

Class A push-Pull Power Amplifier :-



Push pull ckt

→ when a.c signal is applied to the input. when the input signal voltage is positive, the base of transistor T_1 is more positive while the base of transistor T_2 is less possitive.

→ Hence the Collector Current iC_1 of transistor T_1 increases while the collector current iC_2 of T_2 is decreases.

→ Now current flow in opposite direction in two halves of the primary of output transformer. Moreover the flux produced by these current will also be in opposite direction.

→ AS a reasult, the voltage across the load will be induced voltage whose magnitude will be propotional to the difference of collector current i.e $(i_{c_1} - i_{c_2})$.

→ Similarly, fore -ve input signal, the collector current i_{c_2} will be more than i_{c_1}. In this case the voltage developed across the load will agin due to the diff. $(i_{c_2} - i_{c_1})$. AS the $i_{c_2} > i_{c_1}$, the polarity of voltage induced across load will be reversed.

→ The overall opp. reasult in an a.c voltage induced in the secondary of output transformer and hence a.c Powere is delived to load.

The o/p voltage induced in secondary of output transformer is proportional to $(i_{c1} - i_{c2})$

$$v_0 = k \times (i_{c1} - i_{c2}) = k \times 2[I_1 \sin\omega t + I_3 \sin 3\omega t + I_5 \sin 5\omega$$

∴ There is no even harmonic terms, hence all even harmonics are eliminated.

Advantages :-

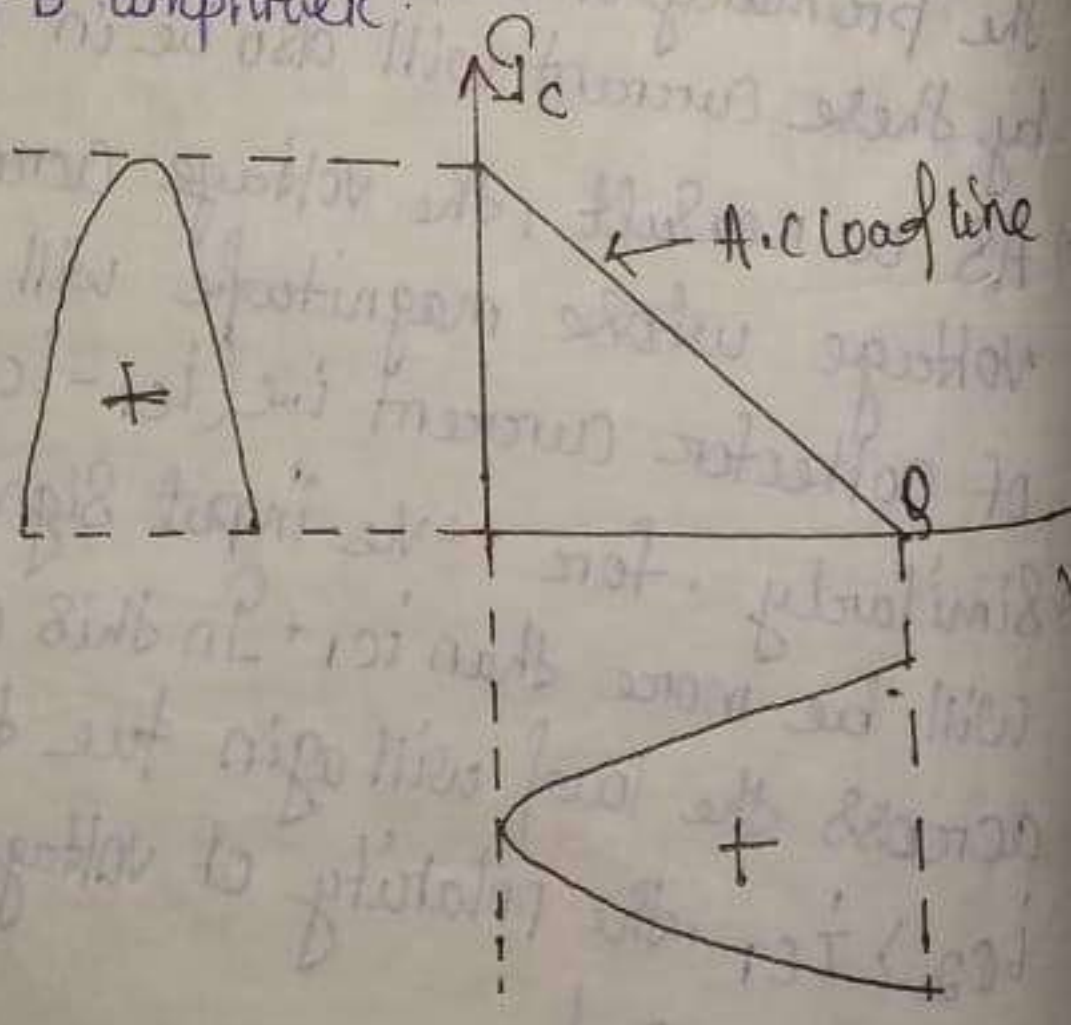
i Even harmonics are absent in the output.
ii High a.c output power is obtained.

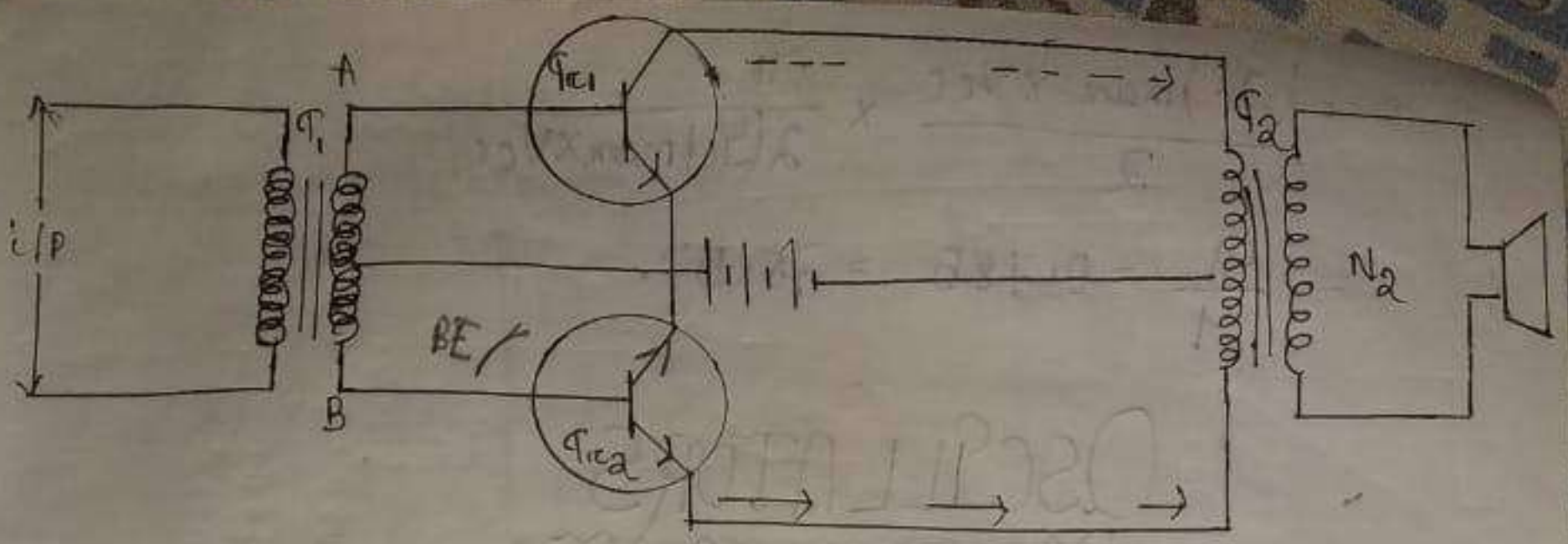
Disadvantages :-

i Two identical transistors are required.
ii Centre tapping is required in transformer.
iii Transformers used are bulky & expensive.

Class B - Push Pull Amplifier :-

→ when the collector current flows only during the positive half cycle of the input signal, the amplifier is called class-B amplifier.





→ During the first half cycle of the signal, end A becomes +ve and end B negative. This will makes the B-E junction of T_{rc_1} is R.B and T_{rc_2} is F.B.

→ The circuit will conduct the current due to T_{rc_2} only and is shown by solid arrows. So in this half cycle the signal is amplified by T_{rc_2} and appears in the lower half of the primary o/p of transformer.

→ In the next half cycle of the signal is T_{rc_1} is F.B and T_{rc_2} is R.B i.e T_{rc_1} conducts and as shown by dotten arrow. Thus the transistor T_{rc_1} will amplify and appears in the upper half of the o/p P-transformer.

→ The center tapped primary of the o/p transformer combine two collector currents to form a sine wave o/p in the second.

→ Due to push-pull B type amplifier, maximum power transformer to the load through the impedance matching.

R_L = Resistance Appearing in primary $= \left(2\frac{N_1}{N_2}\right)^2 \cdot R_L$

N_1 = No. of turns either primary end or centre tapped.

N_2 = Number of sec. turns.

$$\eta_{overall} = \frac{(P_o)_{ac}}{(P_{in})_{d.c}}$$

$$= \frac{(I_C)_{max} \times V_{CC}}{2} \times \frac{\pi}{2(I_C)_{max} \times V_{CC}}$$

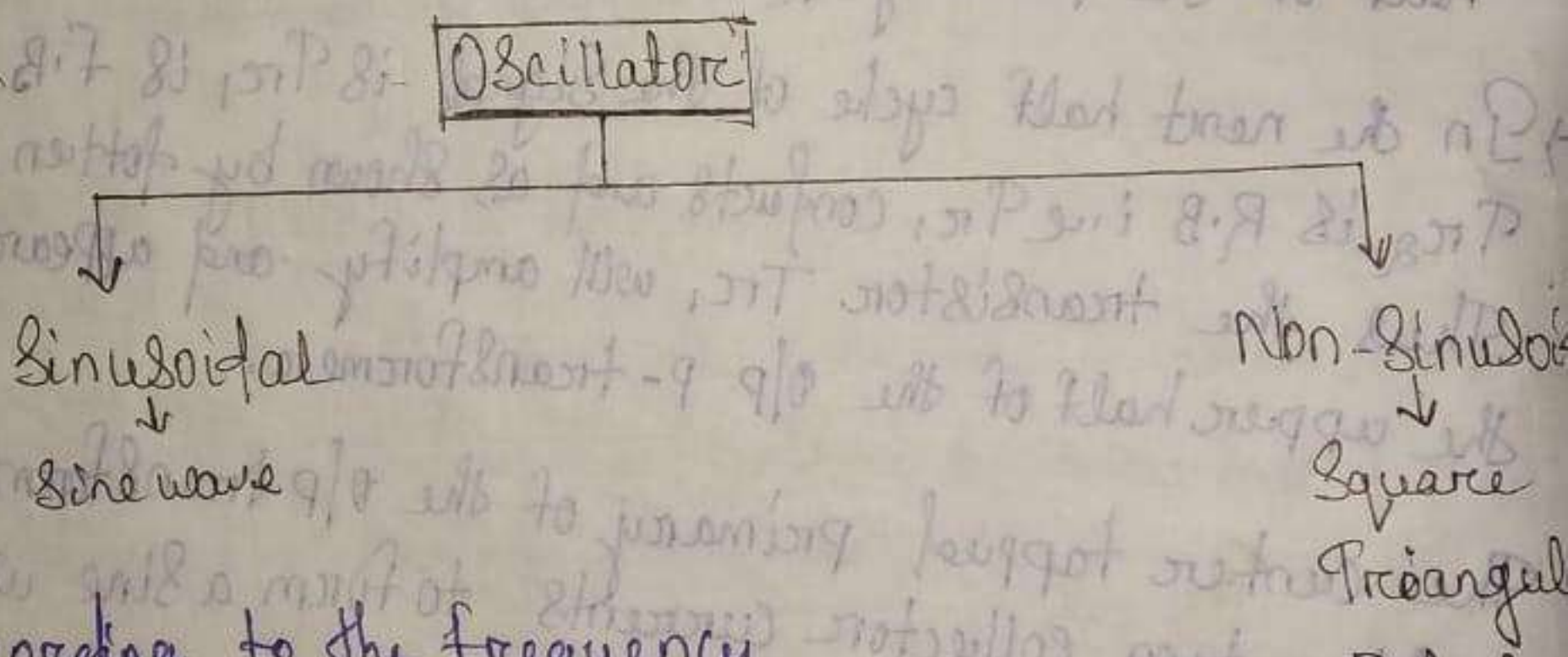
$$= \frac{\pi}{4} = 0.785 = 78.5\%.$$

OSCILLATORS

→ It is an eletronic device which produces Periodic oscillating electrical signal i.e Sine wave/Square

→ Oscillator converts D.C to A.C signal.

→ They are widely used in many electronic devices such as signal broadcasting by radio & television transmiters, computer, RADAR, Clock etc



According to the frequency

i Audio frequency

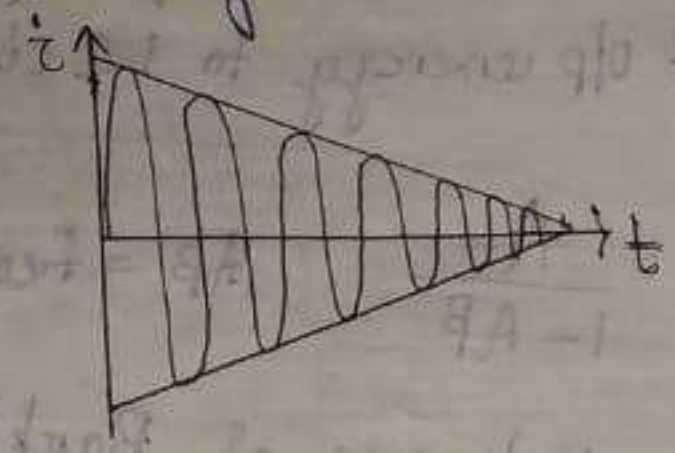
ii Radio frequency.

Types of Sinusoidal Oscillation :-

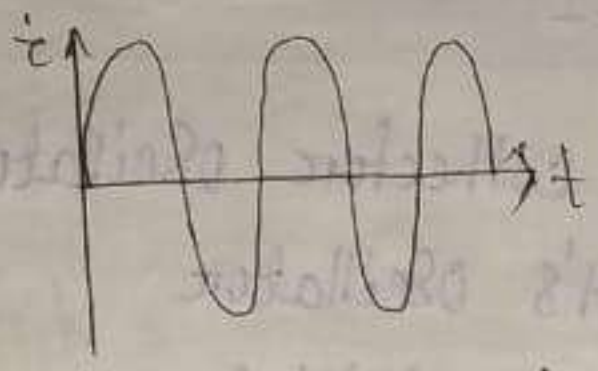
i Damped Oscillation

ii undamped Oscillation.

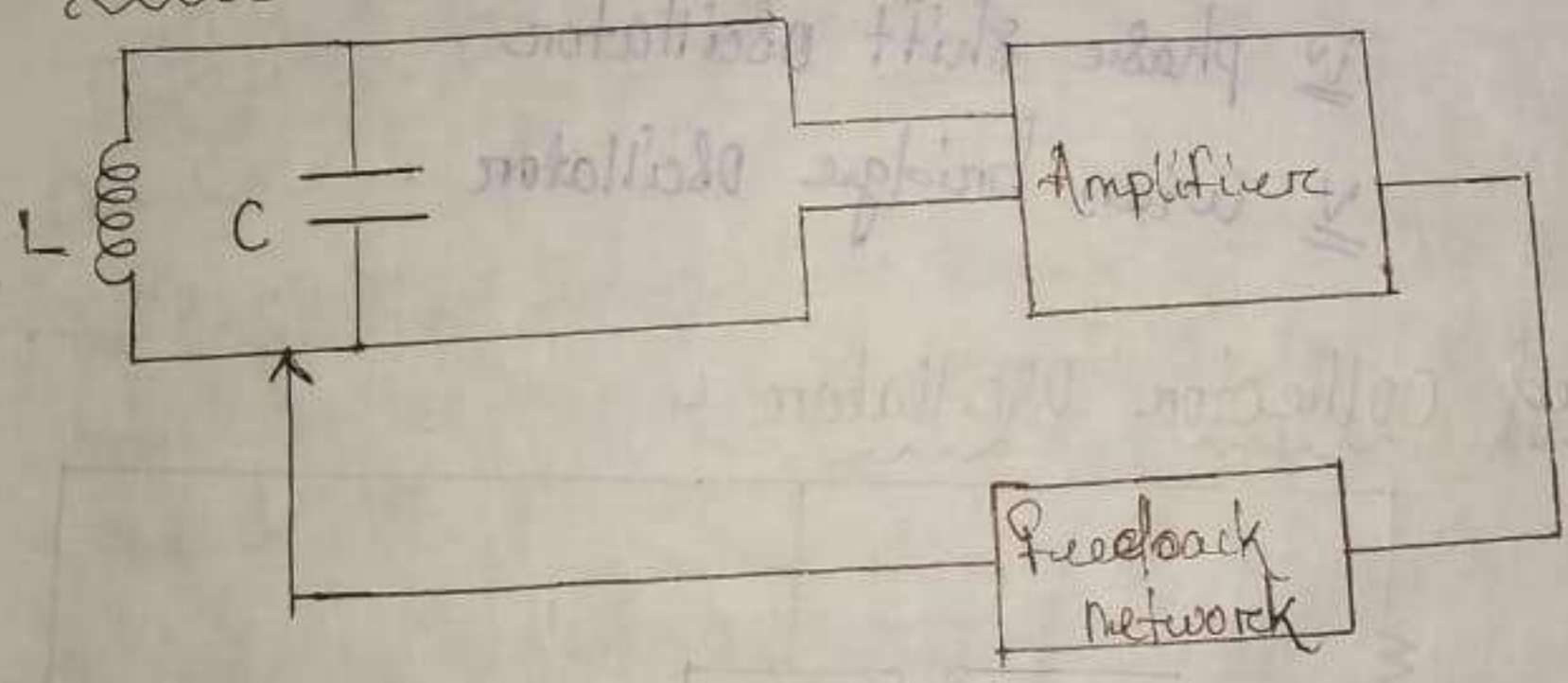
Damped oscillation → The electrical oscilation whose amplitude goes on decreasing with time is called damped oscillation.



Undamped oscillation → The electrical oscillation whose amplitude remain constant with time.



Essential of transistor Oscillator :-



i Tank Circuit → It consist of an inductive coil of inductance (L) connected in parallel with a capacitor of capacitance (C).

→ The frequency of oscillation in the circuit depends upon the value of L and C.

→ The resonance frequency is given by $f_0 = \frac{1}{2\pi\sqrt{LC}}$

ii Amplifier → The function of amplifier is to amplify the oscillation produced by LC circuit. A ampl receives d.c power from battery & converts into a.c sig

→ Transistor increases the output of these oscillation.

Feedback Circuit :- The function of feedback is to transfer a part of o/p energy to LC circuit in proper phase.

$$A_f = \frac{A}{1 - A\beta}$$ $A\beta$ = feedback factor.

$A\beta = 1$ is known as Barkhausen Criterion

Types of Oscillator :-

i. Tuned collector oscillator
ii. Colpitt's oscillator
iii. Hartley oscillator
iv. phase shift oscillator
v. wien bridge oscillator.

Tuned collector oscillator :-

→ It contains tuned circuit L_1-C_1 hence it's name is tuned collectore oscillatore.

→ The frequency of oscillation depends upon the value of L-C. is given by.

$$f_0 = \frac{1}{2\pi\sqrt{L_1C_1}}$$

→ The feedback coil is magnetically coupled L_2-L_1. where L_1 & L_2 is Primary & Secondary transformer.

→ The Capacitore C_E provides low reactant path to the Circuit

→ when the switch 'S' is closed, collectore current starts increasing and charges the capacitore C_1. when the capacitore is fully charged it discharges through coil L.

→ The oscillation induced some voltage in coil L_2 by mutual induction. The frequency of voltage in coil L_2 is depending upon the no. of turns of L_2 and coupling betn L_1 & L_2.

→ The voltage across L_2 is applied betn base and emitter and appears in the amplified from collectore circuit.

Colpitt's Oscillatore

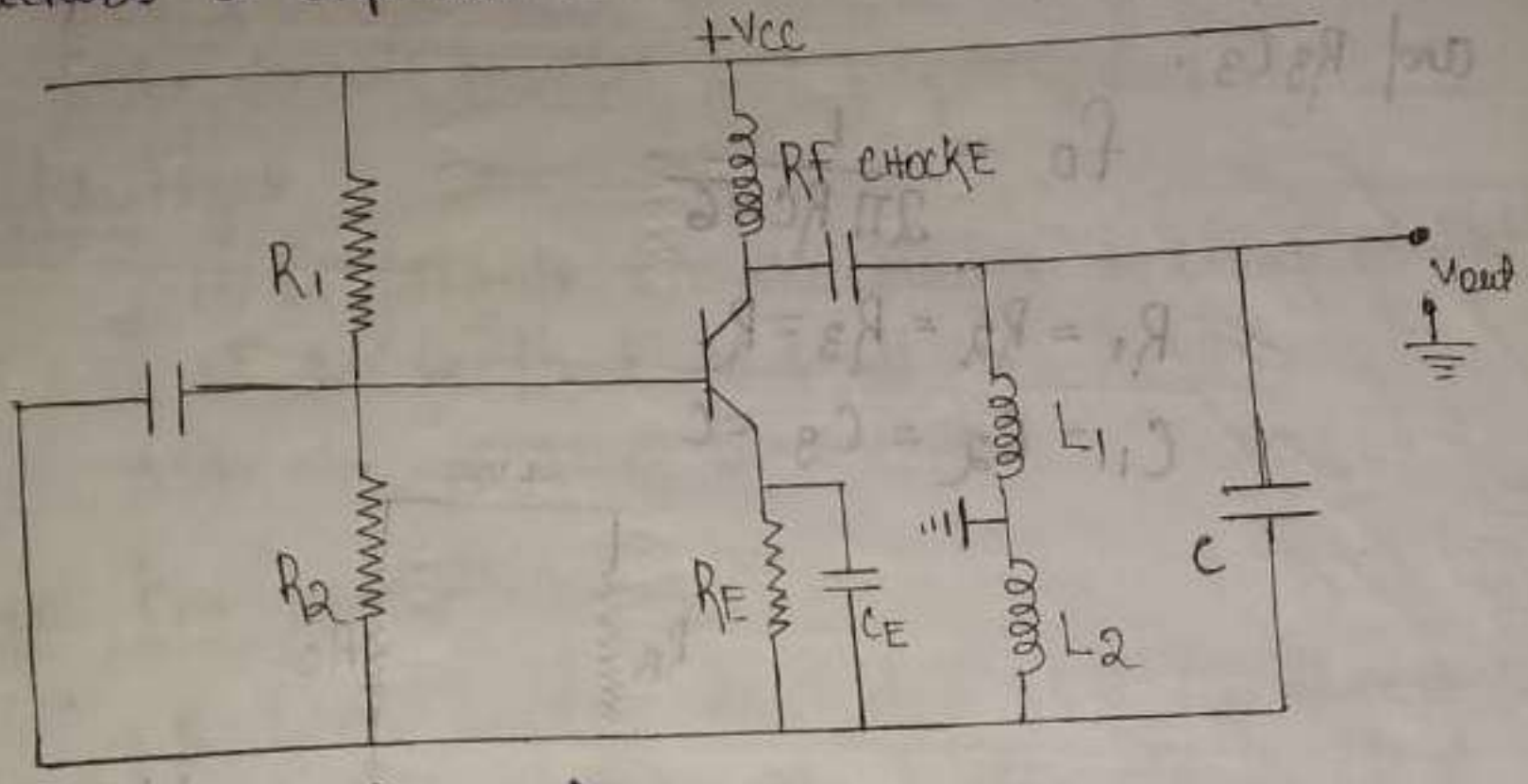
→ It uses two capacitore placed across a common inductore L and the centre of the two capacitore is tapped

→ $f_0 = \frac{1}{2\pi\sqrt{LC_T}}$

→ $C_T = \frac{C_1C_2}{C_1+C_2}$

Hartley Oscillator :-

Here the two inductors L_1 & L_2 are placed across a capacitor C.



$$f = \frac{1}{2\pi\sqrt{CL_T}}$$

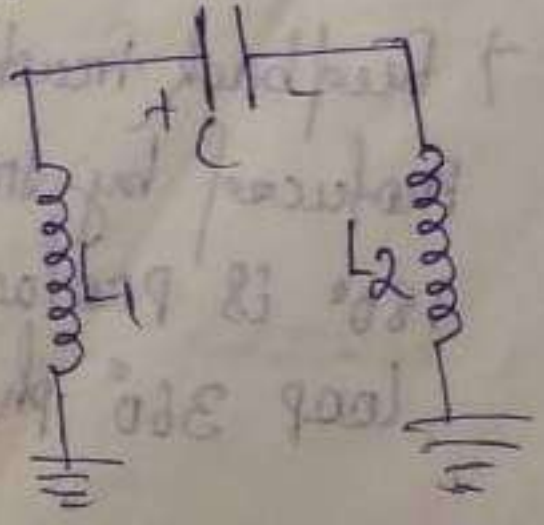
$$L_T = L_1 + L_2 + 2M$$

M = Mutual inductance betn L_1 and L_2.

→ when the circuit is on, the capacitor is charged. when it fully charged it discharged through coil L_1 & L_2

→ The o/p voltage of amplifier appears across L_1 and feedback voltage across L_2. The voltage drop across L_2 is 180° out phase with the voltage developed across L_1.

→ It is easy to see the voltage feedback of L_2 provide (+ve) feedback. A phase shift of 180° is produced by transistor and a further phase shift of 180° is produced by L_1-L_2 voltage divider



→ $M_V = \frac{L_2}{L}$.

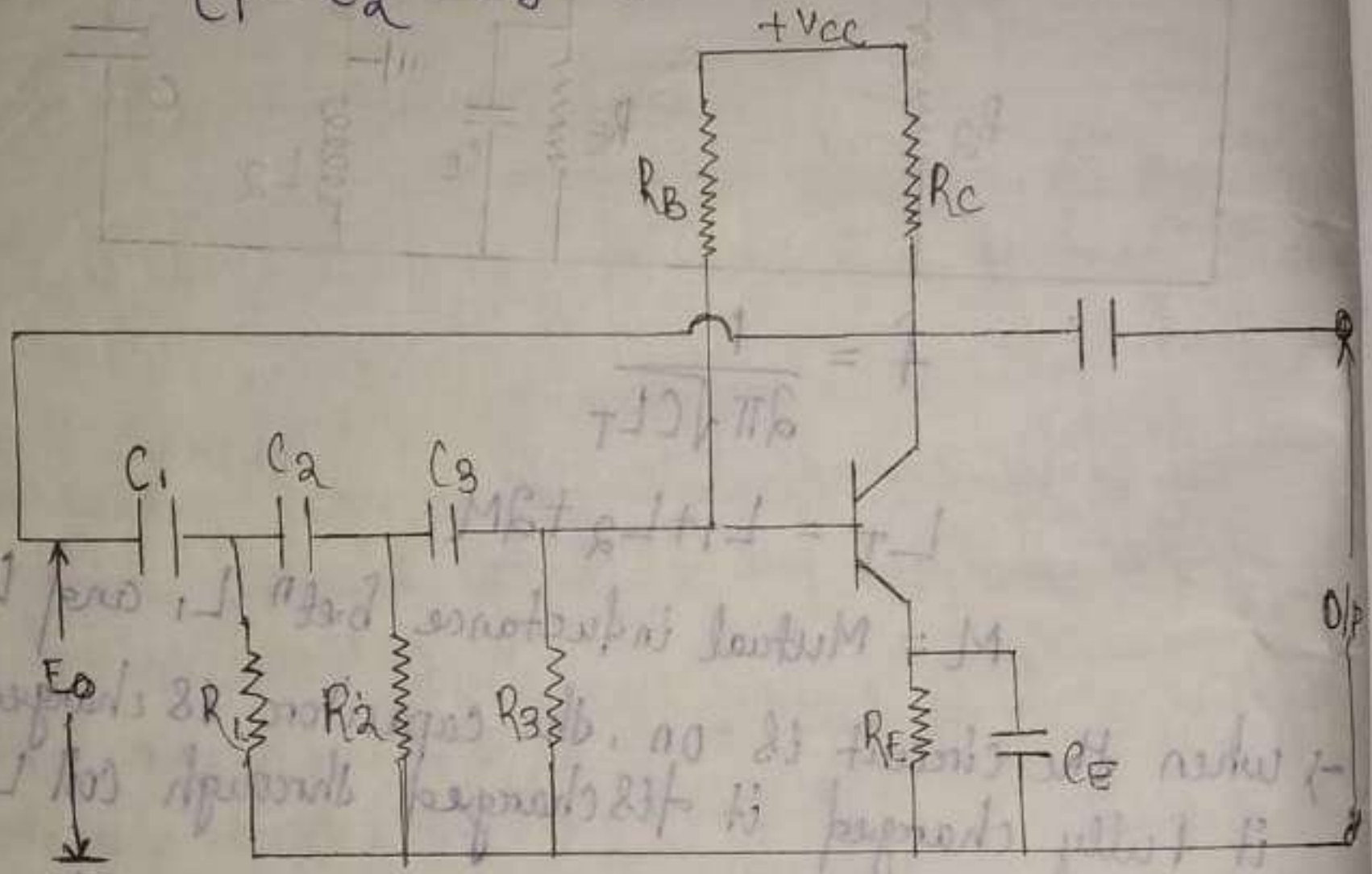
Phase - Shift Oscillator

→ It consist of a amplifier and RC phase shift network. The phase shif consist of three section R_1C_1, R_2C_2 and R_3C_3.

$$f_o = \frac{1}{2\pi RC\sqrt{6}}$$

$$R_1 = R_2 = R_3 = R$$

$$C_1 = C_2 = C_3 = C$$



→ when the circuit is switched on, it produced Oscillations of frequency determined by - The output Eo of the amplifier is feedback to RC feedback network.

→ This feedback network produces a phase shift of 180° and a voltage E_i appears at its output which is applied to transistor amplifier.

→ feedback fraction $m = E_i/E_o$. A phase shift of 180° is produced by transistor Amplifier - A further phase shift 180° is produced by R.C network. Around entire loop 360° phase shift produced.

Advantages :-

→ It does not require transformers / inductors.
→ It can be used to produce very low frequencies.
→ The circuit provides good frequency stability.

Disadvantages :-

→ It is difficult for the circuit to start oscillations as the feedback is small.
→ The circuit gives low output.

Wien Bridge Oscillator :-

→ A wien bridge oscillator is a two stage amplifier with R-C bridge circuit. The bridge circuit has the arms R_1C_1, R_3, R_2C_2 and tungsten lamp Lp.

→ Resistance R_3 and Lp are used to stabilise the amplitude of the o/p. Transistor T_1 serves as an oscillator and amplifier while other transistor T_2 serves as an inverter (180° phase shift).

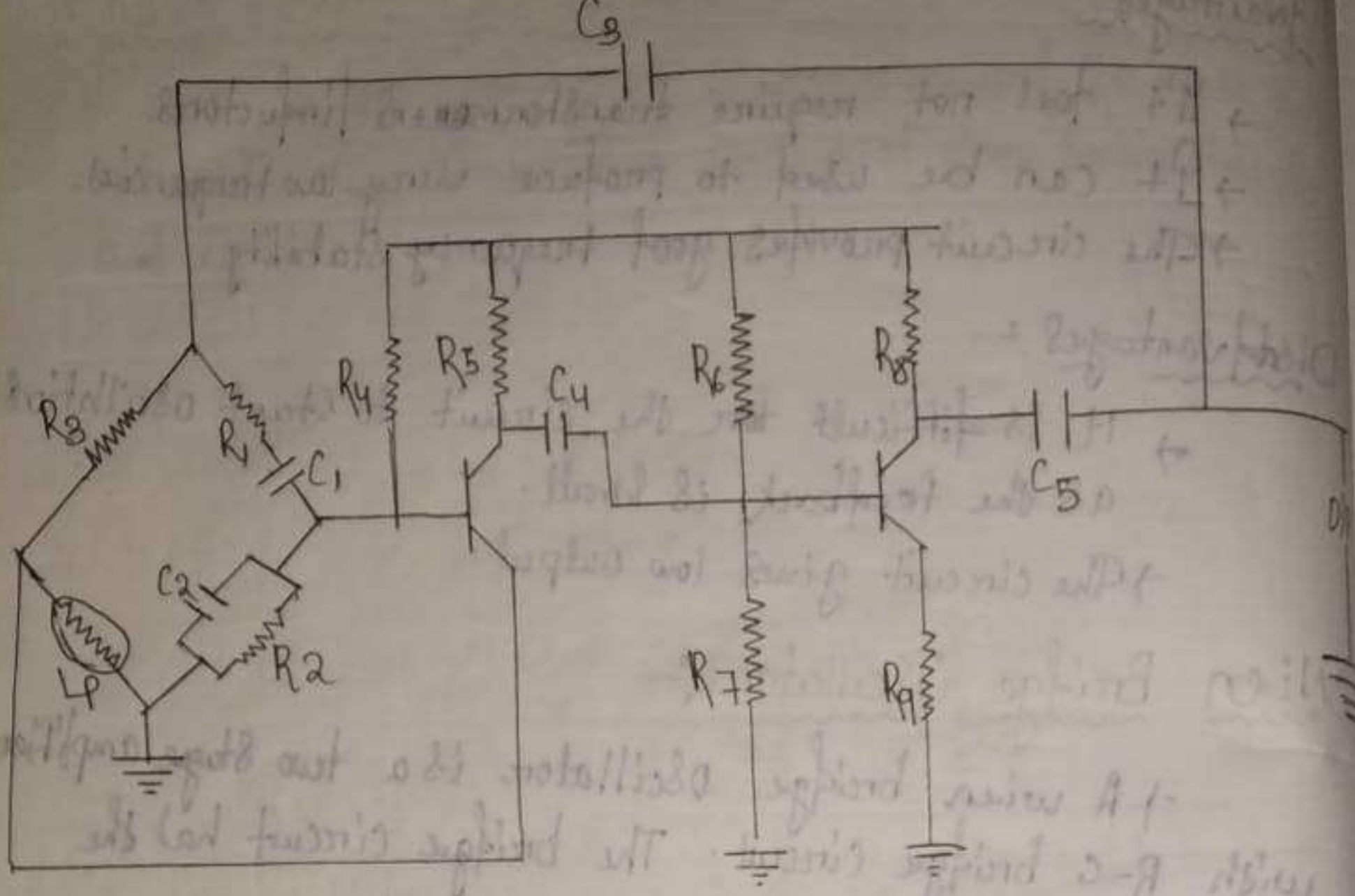
→ The circuit uses both (+ve) & (-ve) feedback. Possitive feedback through R_1C_1 C_2R_2 to the transistor T_1. The negative feedback through voltage divider to the input transistor T_2.

$$f = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$$

If, $R_1 = R_2 = R$

$C_1 = C_2 = C$

$$f = \frac{1}{2\pi RC}$$



→ The two transistors produce a total phase shift of 360° so that proper positive feedback is ensured.

→ The negative feedback in the circuit ensures constant output. This is acheived by the temp. sensitive tungsten lamp Lp. It's resistance increases with current.

→ The amplitude of o/p tends to increase, more current would provide more negative feedback. The result is that the o/p would return to original value.

Advantages → i) It gives constant output
ii) The circuit works quite easily
iii) The overall gain is high because of two

Disadvantages → i) Large no. of component required
ii) Can not generate very high fre

7TH CHAPTER

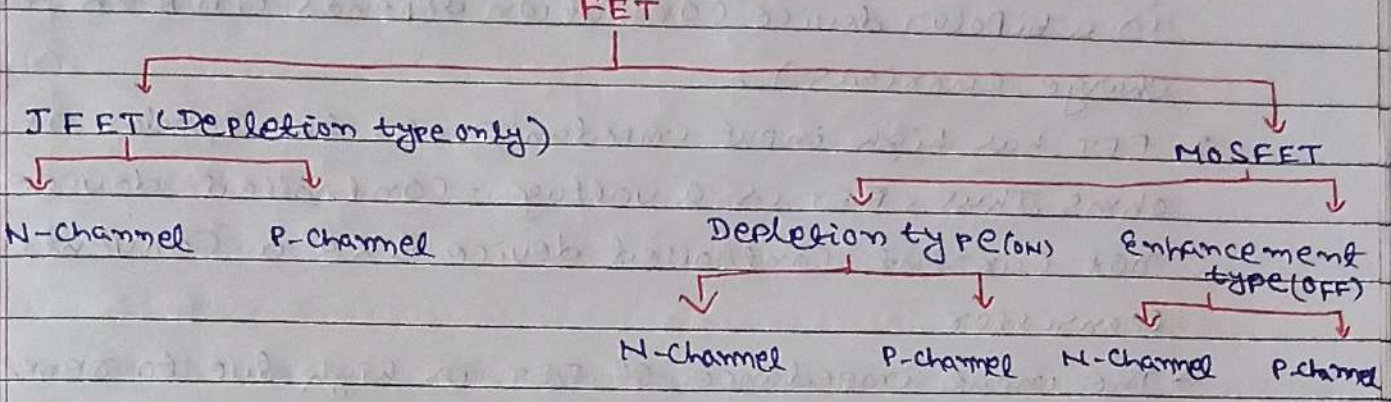
FIELD EFFECT TRANSISTOR

Ch-7 Field effect transistor (FET)

Introduction:-

→ The field-effect transistor (FET) is a three terminal unipolar semiconductor device in which current is controlled by an electric field.

Classification of FET:-



Difference between BJT & FET:-

BJT	FET
1) BJT means Bipolar Junction transistor.	1) FET means field effect transistor.
2) It has three terminals. (i.e. Emitter, base, collector)	2) It has also three terminals. (i.e. Drain, Source, Gate)
3) It is a Bipolar device. (current conduction, by both types of charge carriers, i.e. electron or holes)	3) It is a unipolar device. (current conduction is only due to one type of charge carrier either electron or hole)
4) It is current controlled device.	4) It is a voltage controlled device.
5) BJT has High noise level.	5) FET has low noise level.
6) It has Low input impedance (z) (Due to forward bias)	6) It has high input impedance (z) (Due to reverse bias)
7) In BJT, thermal stability is less.	7) In FET, thermal stability is more.
8) It has shorter life span with low efficiency.	8) It has longer life span with high efficiency.
9) It base on -ve temp. coefficient. (T↑, R↓)	9) It based on +ve temp. coefficient (T↑, R↑)
10) BJT has low power gain (o/p / i/p)	10) FET has high power gain.

Advantages of FET over the conventional transistor:-

1. The FET is a unipolar device, depending only upon majority charge carriers (either electrons in N-channel type or hole in P-channel type).
Ex:- vacuum tube. where as the conventional transistor is a bipolar device (operation depends on both the charge carriers).
2. FET has high input impedance, of the order of 10^{10} to 10^{15} ohms. Thus, FET is a voltage-controlled device and not current controlled device like a conventional transistor.
→ The input impedance of FET is high due to reverse bias at input where as the input impedance of BJT is low due to forward bias.
3. FET is less noisy than conventional transistor.
4. FET is less affected by radiation as compared to conventional transistor.
5. It has better thermal stability.
6. The structure of FET is simpler & it occupies less space.
7. FET has small size, longer life and high efficiency
8. FET has very high power gain.

Disadvantages of FET over conventional transistor:-

1. Transconductance is low and hence the voltage gain is low. In case of transistor transconductance is high, so the voltage gain is high.
2. They are more costly than junction transistor.

Note:- Transconductance = O/P current / i/p. voltage.

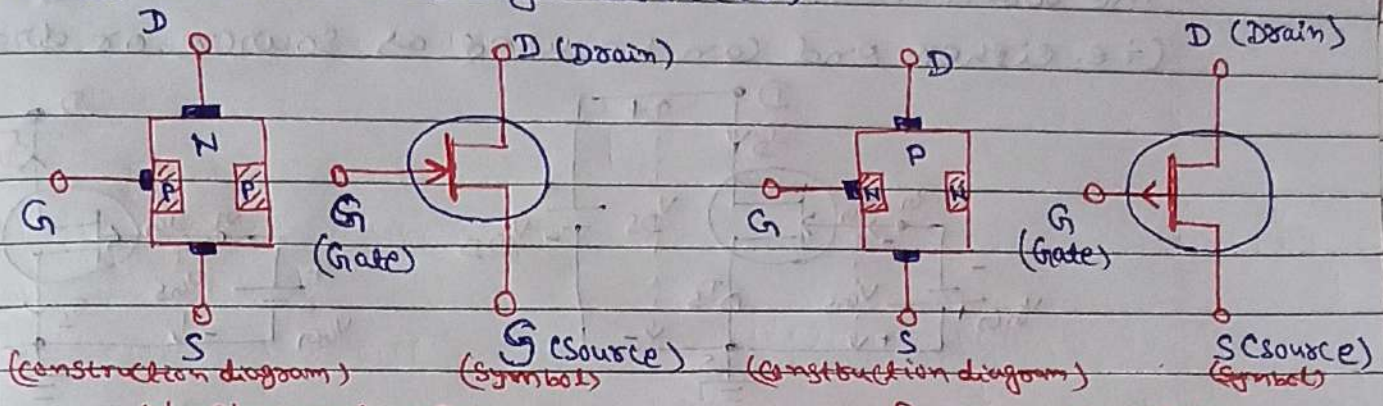
Junction field effect Transistor (JFET)

→ A junction field effect transistor is a three terminal semiconductor device in which current conduction is takes place either by electrons or by holes.

Basic Construction :-

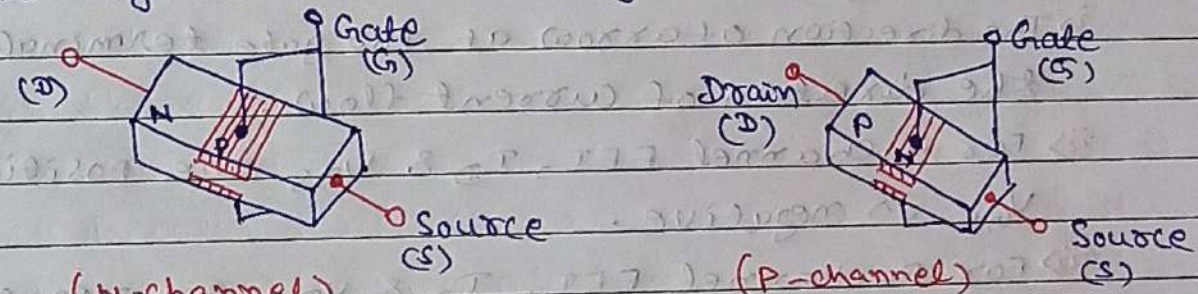
→ JFET are of two types. a) N-Channel JFET b) P-Channel JFET

→ Generally N-Channel is preferred (Due to the dimension & speed of flow of charge carriers).



→ For the construction of N-Channel JFET, a narrow bar of N-type semiconductor material is taken.

→ Now on opposite side of its middle part, two heavily doped P-type regions are formed by diffusion.



→ Similarly for P-channel JFET, a narrow bar of P-type semiconductor material is taken & n-type semiconductor is diffused.

→ Source :- The source (S) is a terminal through which the majority carriers enter into the bar.

→ Drain :- The drain (D) is a terminal through which the majority carriers leave the bar.

→ Gate :- These are two internally connected heavily doped impurity regions which from two P-N Junction. This terminal is known as Gate terminal.

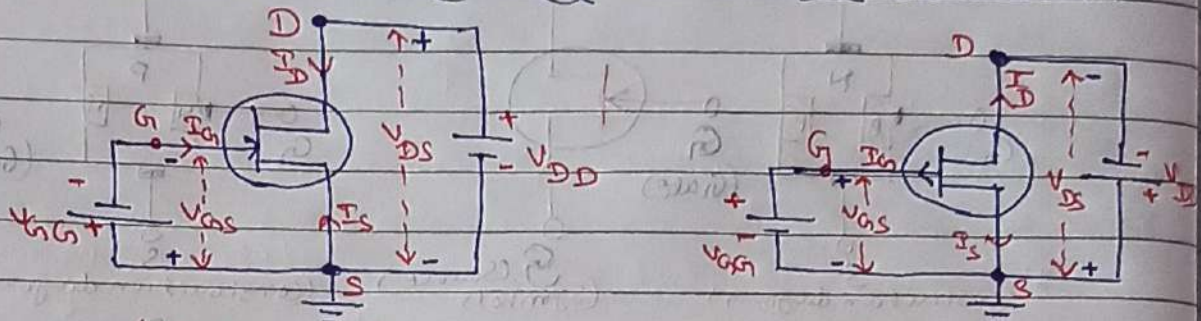
→ Channel :- The space between two gates through which majority carriers pass is known as channel.

→ The source and drain terminals may be interchanged.

Circuit Symbol & notification -:

→ Here the voltage between gate and source is always reverse biased.

→ The drain & source terminals are interchangeable. (i.e. either end can be used as source or drain.



→ V_{DD} = drain supply voltage, V_{DS} = drain to source voltage
V_{GG} = gate supply voltage, V_{GS} = gate to source voltage
I_D = drain current, I_S = source current, I_G = gate current

Some key points -:

i) The direction of arrow at the gate terminal indicates the direction of current flow.

ii) For N-channel FET, I_D & V_{DS} are positive while V_{GS} is negative.

iii) For P-channel FET, I_D & V_{DS} are negative while V_{GS} is positive.

iv) Note -: when a potential difference (V_{DD} or V_{DS}) is applied between source and drain, a current flows from one end to the other end in N-type material which form a sort of channel.

→ This current consists of majority charge carriers which are electrons (N-channel).

→ Similarly, for P-channel JFET, this current consists of majority charge carriers which are holes.

Operation of N-channel JFET:-

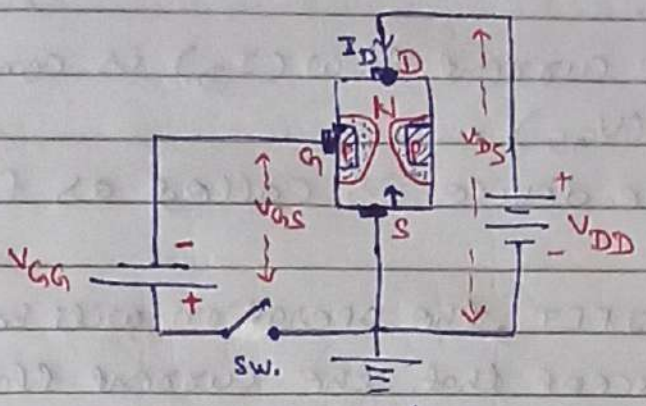


Fig (1) (V_{GG} or $V_{GS}=0$)

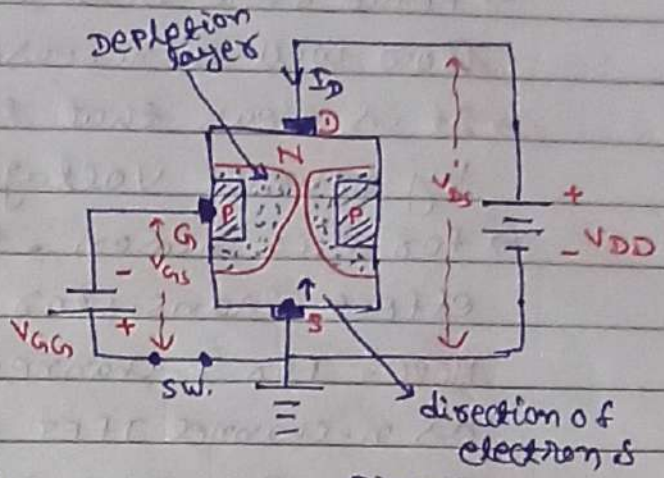


Fig (2)

→ Fig (1) & Fig (2) are the normal circuit diagram of JFET.

→ In fig (1) gate to source voltage ($V_{GS}=0$) & in fig (2) we applied both the supply voltage V_{GG} & V_{DD}.

Case-(1) (V_{GG} or $V_{GS}=0$)

→ When the voltage source ($V_{DD}=V_{DS}$) is applied between drain & source terminal and ($V_{GG}=V_{GS}$) is zero, Depletion layers will be create at the sides of two P-N junction.

→ Here, the drain current (I_D) will flow from drain to source, where as the electron will flow from source to drain.

→ This movement is takes place through a channel.

→ The size of these layers determine the width of the channel & hence current conduction through the bar.

Case-(2)

→ When a reverse voltage (V_{GS}) is applied between the gate & source, the width of depletion layers is increased.

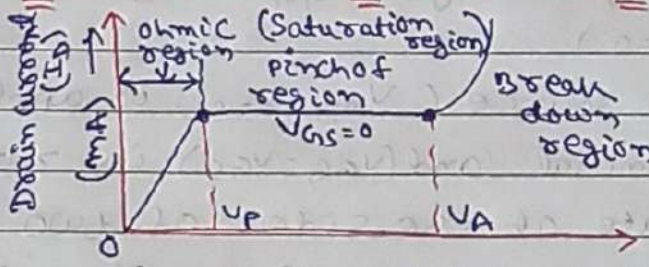
→ This reduces the width of conducting channel, there by increasing the resistance of n-type bar. So that the current flow will decrease.

→ On the other hand, if we decrease the reverse voltage (V_{GS}), then the width of the depletion layers is also decrease.

→ Hence, the width of the conducting channel & current flow will decrease.
→ It is clear that the current flow (I_D) is controlled by reverse voltage (V_{GS}).
→ For this reason, the device is called as field effect transistor.

Note :- For P-channel JFET, the operation will be same as n-channel JFET except that the current flow charge carriers is holes in stead of electron and the polarities of the voltage source V_{GS} and V_{DS} are reversed.

Static characteristic curves of JFET



V_P = Pinch of voltage
V_A = Avalanche Break down voltage

JFET Parameters :-

a) DC drain resistance (R_{DS}) :-
→ This is the static or ohmic resistance of the channel.

$$R_{DS} = \frac{V_{DS}}{I_D}$$

V_{DS} = Drain to Source Voltage
I_D = Drain Current.

b) AC drain resistance (r_d)
→ It is the ratio of change in drain to source voltage (ΔV_{DS}) to the change in drain current at constant gate to Source Voltage (V_{GS})

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$ at constant V_{GS}

c) Transconductance :- (g_{fs}) or (g_m)
→ It is the ratio of change in drain current (ΔI_D) to the change in gate to Source voltage (ΔV_{GS}) at constant drain to Source voltage (V_{DS}).

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$$ V_{DS} = constant

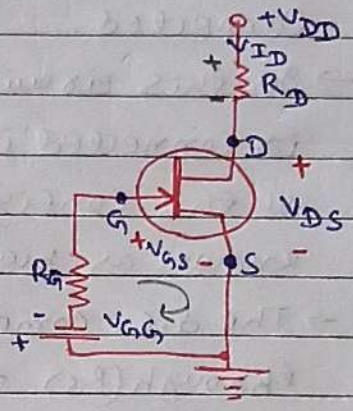
Biasing of FET Circuits :

→ FET Biasing are of 3 types.

a) Fixed-bias configuration b) self-bias configuration

c) voltage divider bias.

Fixed-bias Configuration



→ This is the simplest type of biasing arrangement & is also known as gate bias circuit.

→ A battery (V_{GG}) is used such that its negative is connected to the gate through gate resistance (R_G) and positive is grounded.

→ This battery source ensures that gate-Source junction is reverse-biased.

→ Here, there is no gate current (i.e. $I_G = 0$). So, no voltage drop across (R_G).

→ The zero voltage drop across R_G permit us to replace it by short circuit in case of d.c analysis.

* For d.c analysis, $\boxed{I_G = 0}$ — (i)

Applying KVL to the input circuit, we have

$$-V_{GS} - V_{GG} = 0 \Rightarrow \boxed{V_{GS} = -V_{GG}} \quad \text{— (ii)}$$

* The drain current is given by $\boxed{I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2}$ — (iii)

I_D = Drain current.

where I_{DSS} = Drain to Source Saturation current.

V_P = pinch off voltage, V_{GS} = Gate to Source voltage

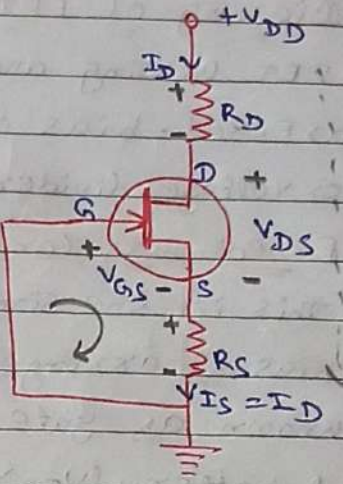
* Applying KVL to output circuit,

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$\Rightarrow \boxed{V_{DS} = V_{DD} - I_D R_D} \quad \text{— (iv)}$$

→ Since V_{GG} is fixed value of d.c supply and the magnitude of V_{GS} is also fixed, hence the circuit is named as fixed bias circuit.

Self-Bias Configuration



→ The circuit required only one supply voltage (i.e. drain supply V_{DD}) and no gate supply (V_{GG}) is connected.

→ In this circuit, a Resistor (R_S) is connected in the Source leg of the configuration. This is known as bias resistor.

→ The d.c. component of drain current (I_D) flowing through (R_S) makes a voltage drop across resistor (R_S). This voltage drop makes the gate to source reverse voltage required for FET operation.

* Applying KVL to the input circuit, we have

$$-V_{GS} - I_S R_S = 0$$

$$\Rightarrow \boxed{V_{GS} = -I_D R_S} \quad (\because I_S = I_D) \quad -(i)$$

* The drain current is given by

$$\boxed{I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2} \quad -(ii)$$

* Now Applying KVL to output circuit, we have

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$$

$$\Rightarrow V_{DS} = V_{DD} - I_D R_D - I_S R_S \quad (\because I_S = I_D)$$

$$\Rightarrow V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$\Rightarrow \boxed{V_{DS} = V_{DD} - I_D (R_D + R_S)} \quad -(iii)$$

Voltage Divider Bias :-

→ The name voltage divider is given due to the fact that resistor R_1 and R_2 from a voltage divider across drain supply V_{DD}.

→ The voltage developed across R_2 provides the necessary bias.

→ The gate voltage (V_G) is given by

$$\boxed{V_G = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)} \quad -(1)$$

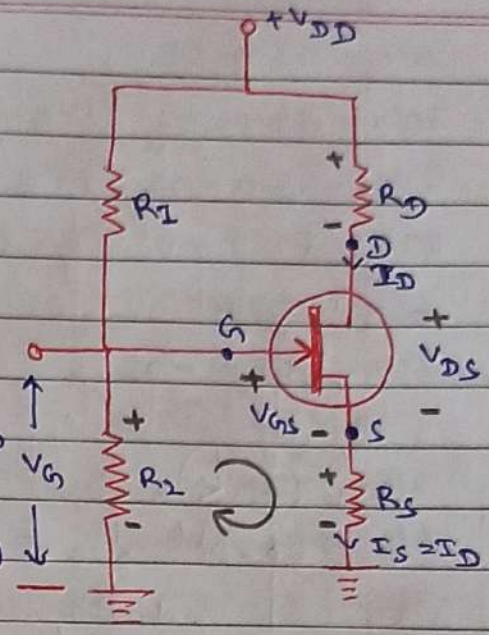
* Applying KVL to the input circuit,

$V_G - V_{GS} - I_S R_S = 0$

$\Rightarrow \boxed{V_{GS} = V_G - I_D R_S}$ — (2) $(\because I_S = I_D)$

then $I_D R_S = V_G - V_{GS}$

$\Rightarrow \boxed{I_D = \frac{V_G - V_{GS}}{R_S}}$ — (3)



* Now Applying KVL to the output circuit,

$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$

$\Rightarrow V_{DS} = V_{DD} - I_D R_D - I_S R_S \quad (\because I_S = I_D)$

$\Rightarrow V_{DS} = V_{DD} - I_D R_D - I_D R_S$

$\Rightarrow \boxed{V_{DS} = V_{DD} - I_D (R_D + R_S)}$ — (4)

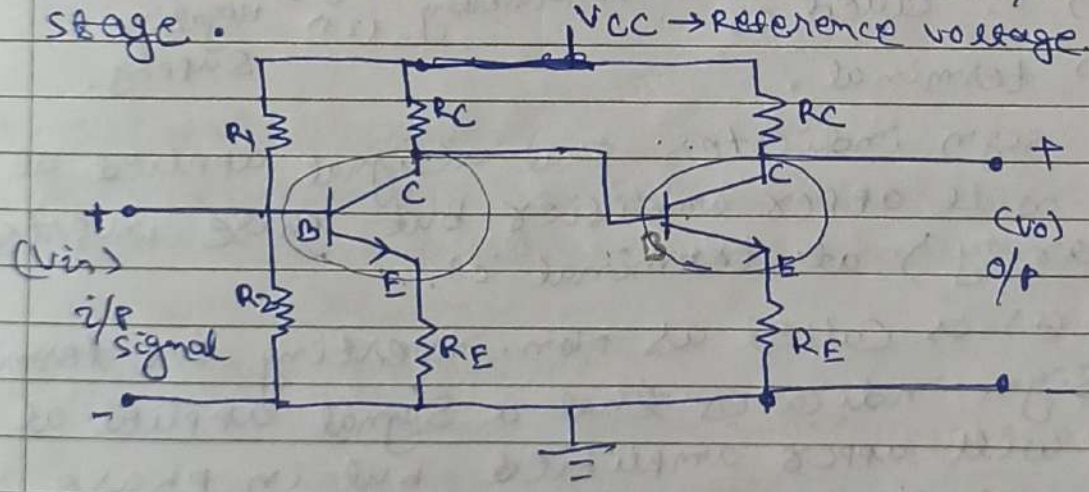
By determine the value of I_D & V_{DS}, we can get the operating point $(Q) = (I_D, V_{DS})$.

Date .....

Expt. No. CP-4 OPERATIONAL AMPLIFIER Page No. .....

* The operational amplifier is a direct-coupled, high gain negative feedback amplifier.
* They are made with different internal configurations in linear ICs.
* The operational amplifier was originally used for the d.c. amplifiers which perform mathematical operations as summation, subtraction, integration & differentiation in analog computer.
* Analog computer -: It is a type of comp. that uses the continuously changeable aspects of physical phenomena such as electrical, mechanical model for problem solving.
* Direct-coupled amplifier -: (DC amplifier)

→ It is a type of amplifier in which the o/p of one stage of the amplifier is coupled to the i/p of the next stage.



* Now a days, OP-AMPS are used as voltage regulator, phase shift and oscillator circuits, pulse generators, square wave generator etc.
* Frequency range of OP-AMP -: 0 Hz to 1 MHz
* OP-AMP can be used to amplify d.c signal as well as A.C signal.

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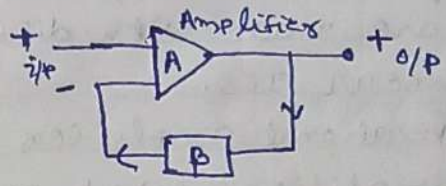
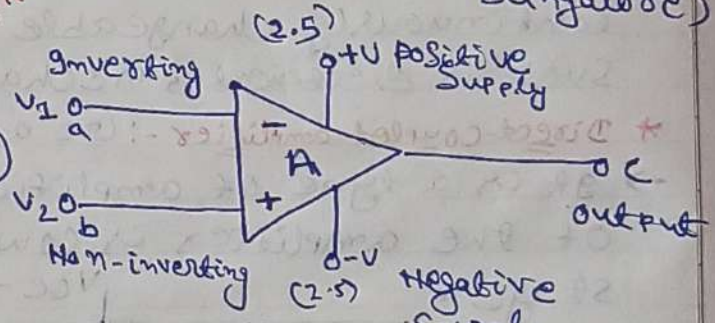
* **Positive feedback** :- when feedback voltage is applied to increase the i/p signal is called +ve feedback. (Distrotion & instatability)
* **Negative feedback** :- when feedback voltage is applied to decrease the i/p signal is called -ve feed back. (gain stability, reduction of distortion)



Advantages of OP-AMP :-

* Small size, reduced cost, high reliability, less power consumption etc. Ex:- CA741 OPAMP (manufactured by BEL, Bangalore)

Circuit Symbol of an OP-AMP



* The OP-AMP has two i/p terminals and a single o/p terminals.
* Terminal 'a' (-) is called as inverting i/p terminal.

→ Here (-)ve sign indicates that a signal applied at the terminal 'a' will apper amplifier but phase inverted (opposite polarity) at terminal 'c'.

→ Terminal 'b' (+) is called as Non-inverting i/p terminal.

→ Here (+)ve sign indicates that a signal applied at the terminal 'b' will apper amplified but in phase (same polarity) at the terminal 'c'.

→ The two D.C sources, (+V and -V) are required for the biasing of OP-AMP. (Biasing :- Steady state cond^n, where no. signal is applied)

→ These voltages are equal in magnitude with opposite polarities.

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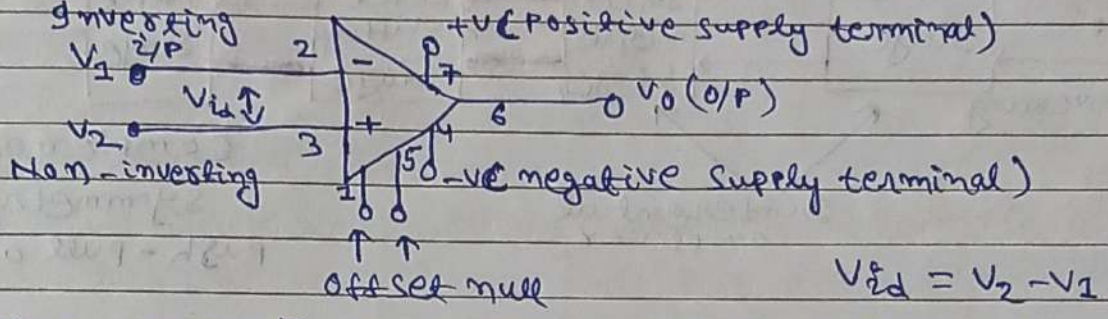
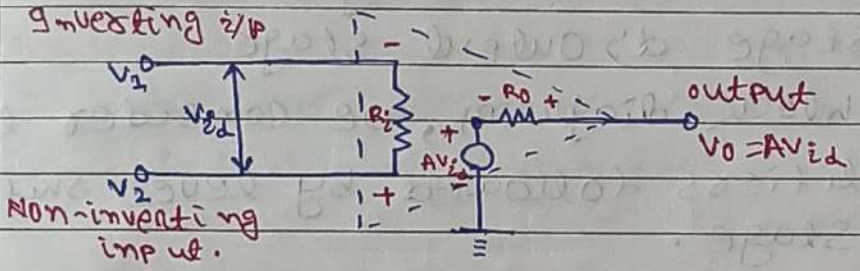
Circuit Symbols of CA 741 OP-AMP



$V_{id} = V_2 - V_1$

Offset null condⁿ :- Here the o/p should be 0 V when there is no difference betⁿ its inputs (i/p are same)

Equivalent circuit of OP-AMP :-



* V_1 = voltage at the inverting terminal
  V_2 = voltage at the non-inverting terminal
  V_{id} = difference of two input voltage ($V_2 - V_1$)
  R_i = i/p resistance
  R_0 = o/p resistance
  AV_{id} = equivalent Thevenin voltage source.
* Here the output voltage is directly proportional to the algebric difference betⁿ the two i/p voltages.
* The gain of the amplifier (A) = $\frac{\text{Output}}{\text{Diff. betⁿ two i/p signals.}}$

$$\Rightarrow A = \frac{V_0}{V_2 - V_1} = \frac{V_0}{V_{id}}$$

In case of Ideal OP-AMP

* $R_i = \infty$, $R_0 = 0$, $A = \infty$ $\Rightarrow$ $\boxed{V_0 = A V_{id}}$

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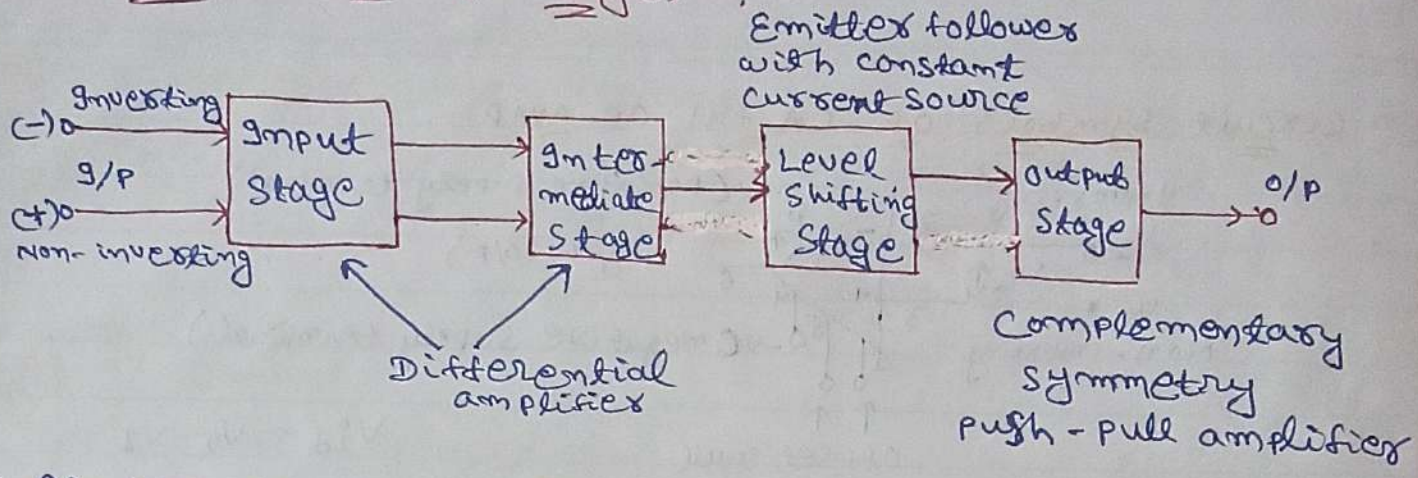
Operational amplifier stages -:



* OP-AMP is a multi-stage circuit it consists of four stages.

a) Input stage b) Intermediate stage
c) level shifting stage d) Output stage

* In the above block diagram, we consider two differential amplifiers followed by level shifter and an output stage.

(Differential amplifier -: It is a type of electronic amplifier that amplifies the difference betⁿ two input voltages and provided output voltage.

a) Input Stage -:

→ The input stage is a dual-input, balanced O/P differential amplifier.

→ The function of differential amplifier is to provide most of the voltage gain to OP-AMP.

→ The differential amplifier in the input stage rejects the common noise signals present at the input terminals and amplifies only the difference between the input signals.

Note :- OPAMP uses direct coupling method, therefore DC voltage level at the emitter terminal rises from stage to stage.

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b) Intermediate Stage :-

→ The intermediate stage is a dual input, unbalanced output differential amplifier.

→ This is driven by the output of first stage and is used to provide some additional gain.

→ There is a direct coupling between the first two stages. So, the d.c level at the output of this stage is well above the ground level.

c) Level Shifting stage :-

~~This circuit~~

→ Here we used the level shifter circuit. This is an emitter follower using constant current source.

→ The function of level shifter is to shift the d.c level at the output of intermediate stages downwards to zero volt with respect to ground.

d) Output Stage :-

→ The output stage is generally push-pull amplifier.

→ Its function is to increase large output voltage swing capability, large output current swing capability of the amplifier and to provide low output resistance.

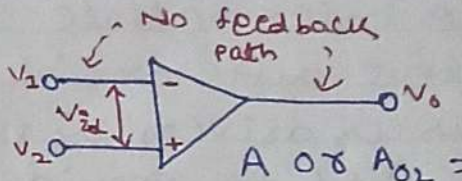
(* Output voltage swing :- It is the max^m positive or negative o/p voltage that can be obtained without wave clipping.)

(* Push-pull amplifier :- It is a type of electronic ckt that uses a pair of active devices that alternately supply current or absorb current from a load.)

Teacher's Signature : _____

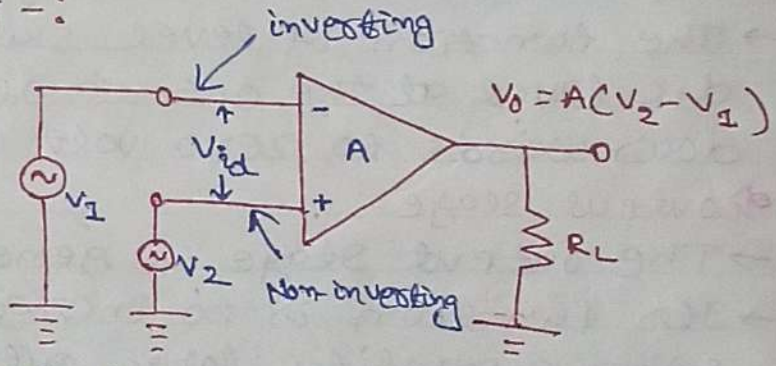
Open-loop OP-AMP Configurations -:

* The term open-loop indicates that there is no feedback path from output side to the input side of the OP-AMP.
* In this diagram, the maximum possible open-loop voltage gain (A or A_{OL}) is 20000.



* There are three open loop configuration.
a) Differential amplifier.
b) Inverting amplifier.
c) Non-inverting amplifier.
* These configurations are based on the numbers of inputs used and the terminal to which the input is applied.

Differential amplifier -:



* In this figure, V_1 and V_2 are signals applied to inverting and non-inverting terminals respectively.
* V_1 & V_2 may be either A.C or d.C as OP-AMP can amplify both types of signals.
* Here, the source resistance are not considered because they are very small in comparison with the very high input resistance of OP-AMP.
* As the OP-AMP amplifies the difference between two input signals, hence this configuration is called as differential amplifier.
* Output voltage $\boxed{V_o = A V_{id} = A(V_2 - V_1)}$ $A = \frac{V_o}{V_{id}}$ where A = large signal voltage gain or open loop gain
* Here the polarity of the output voltage depends on the difference of input voltage.

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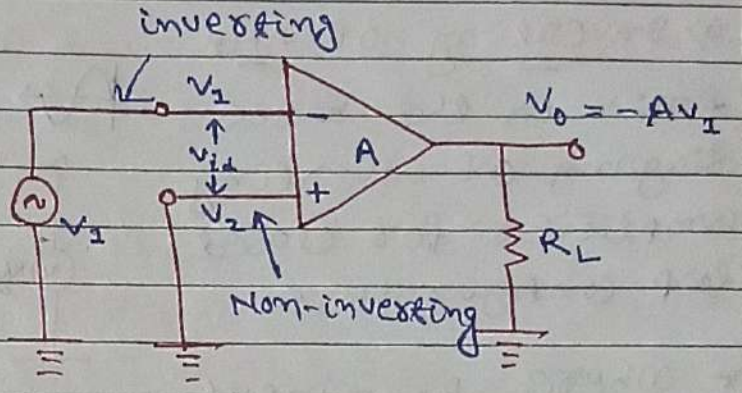
Inverting Amplifier :-

* In this diagram, the input signal is applied to the inverting input terminal and the non-inverting terminal is grounded (i.e. $V_2 = 0$)



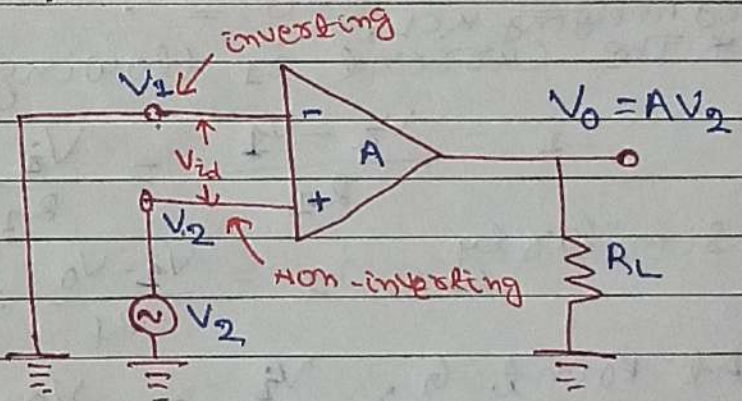
* So the output voltage $V_0 = AV_{id} = A(V_2 - V_1)$

or $\boxed{V_0 = -AV_1}$

* The negative sign indicates that the output voltage is 180° out of phase with respect to input voltage.
* Here the polarity of output voltage is changed with respect to input voltage.

Non-inverting Amplifier :-

→ In this diagram, the input signal is applied to the non-inverting input terminal of the OP-AMP and the inverting input terminal is grounded (i.e $V_1 = 0$).



* So the output voltage $V_0 = AV_{id} = A(V_2 - V_1)$

or $\boxed{V_0 = AV_2}$

* The positive sign indicates that the output voltage is inphase with respect to the input voltage.
* Here, the input signal is amplified by gain (A) without change in polarity.

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Concept of virtual ground

Figure (17·13) shows the inverting amplifier with virtual ground.

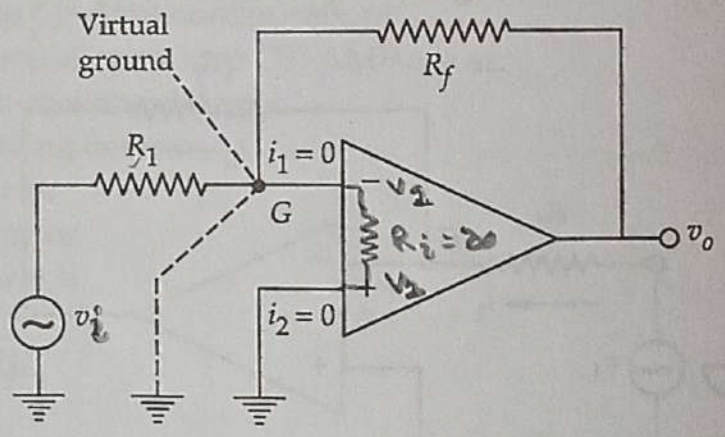


Fig. 17·13 Inverting amplifier with virtual ground

Let us explain the concept of virtual ground. When at any point of the circuit, the potential becomes the same as that on ground (the point is on ground potential), although physically no path for current from that point to ground actually exist, the point is said on ground potential. The point G in fig (17·13) is on ground potential.

The open-loop gain is given by

$$A = \frac{v_0}{v_{id}} = \frac{v_0}{(v_2 - v_1)}$$

$$\therefore \quad (v_2 - v_1) = \frac{v_0}{A} = \frac{v_0}{\infty} \qquad (\because \text{for ideal OP-AMP, } A = \infty)$$

or $$(v_2 - v_1) = 0 \text{ or } v_2 = v_1$$

Therefore, the potential difference between two terminals is zero. In inverting amplifier, the non-inverting terminal is grounded *i.e.*, $v_2 = 0$.

From eq. (1), $$v_0 = 0 \qquad (\because v_2 = 0)$$

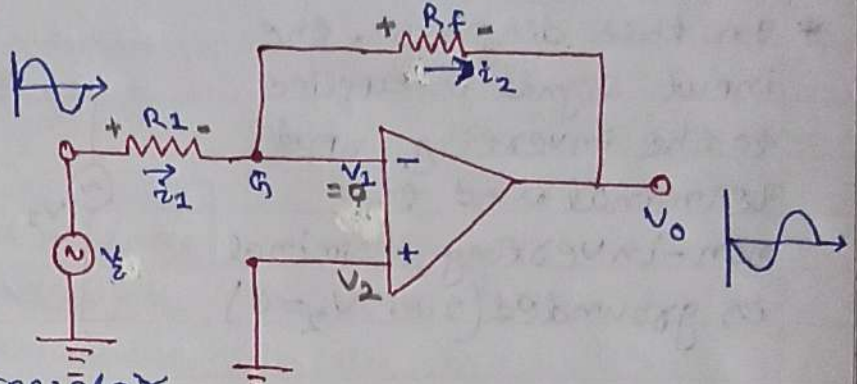
So, point G is on virtual ground.

Closed loop OP-AMP Configurations -:

* The term closed-loop indicates that there is a feedback path from output side to the input side of the OP-AMP.

a) Inverting OP-AMP -:

* This is the basic diagram of inverting amplifier for closed loop configuration.



* where R_1 = input resistor, V_o = output voltage
R_f = feedback resistor, V_i = input voltage

* In this mode of operation, the positive input terminal of the amplifier is grounded & the input signal is applied to the negative input terminals.
* The point 'G' is called as summing point because the output is added to the input at point 'G'.

Expression for gain -:

By applying KVL;

* The current i_1 flowing through point 'G' is given by

$$i_1 = \frac{V_i - V_1}{R_1} = \frac{V_i}{R_1} \quad (\because G \text{ is at ground potential } V_1 = 0)$$

Similarly, $i_2 = \frac{V_1 - V_o}{R_f} = \frac{-V_o}{R_f}$

Apply KCL → $i_1 - i_o = 0 \Rightarrow i_1 = i_2$

At point G, $\Rightarrow \frac{V_i}{R_1} = \frac{-V_o}{R_f}$

* The ratio of output voltage(V_o) and input voltage(V_i) is known as the closed loop gain.

$$A_V = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

* The negative sign signifies that the output voltage is inverted with respect to input voltage.

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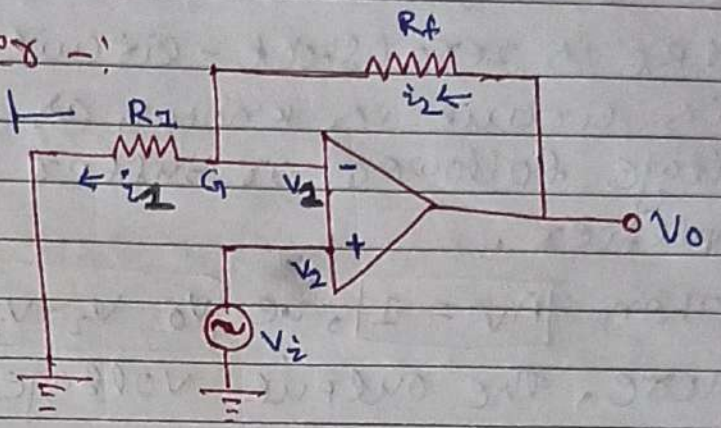
Non-inverting amplifier :-

* This is the basic diagram of non-inverting amplifier for closed loop configuration.
* In this mode of operation, the negative input terminal of the amplifier is grounded & the input signal is applied to the positive input terminals.



Expression for gain :-

* The values of currents i_1 and i_2 are given as (By applying KVL)

$V_i - i_1 R_1 = 0$

$\Rightarrow i_1 = \frac{V_i}{R_1}$ and $i_2 = \frac{V_o - V_i}{R_f}$ $(V_o - R_f i_2 - V_i = 0)$

$(V_1 = V_2 = V_i)$

Applying Kirchhoff's 1st law (KCL) at point G, we get

$(-i_1) + i_2 = 0$

$\Rightarrow \frac{-V_i}{R_1} + \frac{V_o - V_i}{R_f} = 0$

$\Rightarrow \frac{V_o}{R_f} = \frac{V_i}{R_1} + \frac{V_i}{R_f}$

$\Rightarrow \frac{V_o}{R_f} = V_i \left(\frac{1}{R_1} + \frac{1}{R_f} \right)$

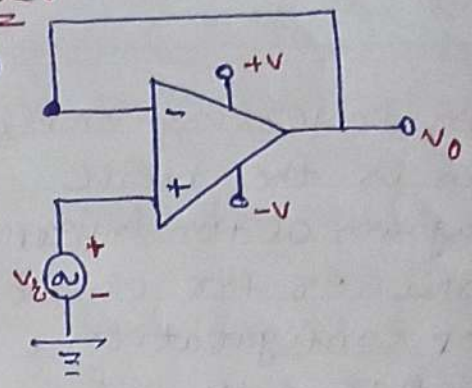
$\Rightarrow \frac{V_o}{R_f} = V_i \left(\frac{R_1 + R_f}{R_1 R_f} \right)$

$\Rightarrow \frac{V_o}{V_i} = \cancel{R_f} \left(\frac{R_1 + R_f}{R_1 \cancel{R_f}} \right) = \left(1 + \frac{R_f}{R_1} \right)$

$\Rightarrow \boxed{A_V = 1 + \frac{R_f}{R_1}}$

Voltage follower or buffer Amplifier

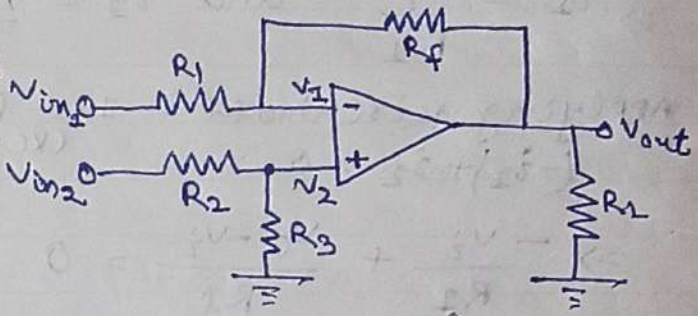
* If R_1 is infinite (open-circuit) and R_f is zero (short-circuit), this circuit is known as voltage follower or buffer amplifier.



* Then $\boxed{A_V = 1}$, i.e. $\boxed{V_o = V_2 = V_i}$
* Here, the output voltage is equal and in-phase with the input i.e. OP-AMP circuit acts as a voltage follower.
* It is required when a signal from high-impedance source is to be amplified and no signal current is to be drawn.

Differential amplifier :-

* A differential amplifier is a circuit which amplifies the difference between two voltages.



* Voltages are applied at both the input terminals of OP-AMP and their amplified difference appears at the output terminal.
* Such a circuit is required when neither of the input lines are grounded.

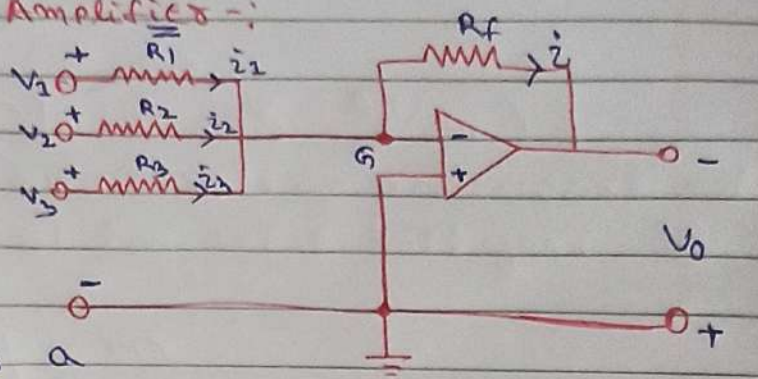
$$\boxed{A_V = -\frac{R_f}{R_1}}$$

A_V = voltage gain.

OPAMP

CP-8

Adder or Summing Amplifier :-



→ Summing Amplifier circuit used in Analog computer.

→ It has 3 input Summing circuit.

→ The circuit provides a means of algebraically summing three input voltages, each Multiplied by a constant gain factor.

→ In this circuit, G is a virtual ground and the output voltage is phase inverted.

→ Here, the different current are given by

$V_1 = i_1 R_1$, $V_2 = i_2 R_2$, $V_3 = i_3 R_3$

$\Rightarrow \boxed{i_1 = \frac{V_1}{R_1}}$ $\Rightarrow \boxed{i_2 = \frac{V_2}{R_2}}$ $\Rightarrow \boxed{i_3 = \frac{V_3}{R_3}}$ and $-V_0 = i R_f$

$\Rightarrow \boxed{i = \frac{-V_0}{R_f}}$

Apply KCL at point 'G', we get

$i_1 + i_2 + i_3 - i = 0 \Rightarrow i_1 + i_2 + i_3 = i$

$\Rightarrow \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{-V_0}{R_f}$

$\Rightarrow V_0 = -R_f \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right]$

$\Rightarrow V_0 = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$ ——— (i)

Consider $\frac{R_f}{R_1} = K_1$, $\frac{R_f}{R_2} = K_2$, $\frac{R_f}{R_3} = K_3$ & $\frac{R_f}{R} = K$

$\Rightarrow V_0 = -[K_1 V_1 + K_2 V_2 + K_3 V_3]$ —(ii)

Case-1 If $\boxed{R_1 = R_2 = R_3 = R}$

Put the value in Eqn (i)

$\Rightarrow V_0 = -\left[\frac{R_f}{R} V_1 + \frac{R_f}{R} V_2 + \frac{R_f}{R} V_3 \right] = -\frac{R_f}{R} [V_1 + V_2 + V_3]$ —(iii)

Case-2 If $\boxed{R_f = R}$

Put the value in Eqn (iii)

$\Rightarrow V_0 = -[V_1 + V_2 + V_3]$ —(iv)

Case-3 If $\boxed{\frac{R_f}{R} = \frac{1}{n}}$ n = no. of inputs.

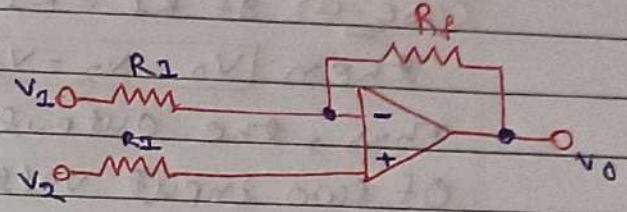
put the value in Eqn (iii)

$$\boxed{V_o = -\frac{1}{3}[V_1 + V_2 + V_3]} \quad -(V)$$

→ In this case, the output is equal to the average of the three inputs.

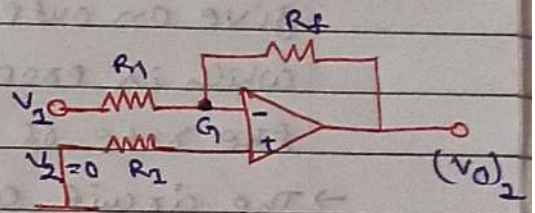
Subtractor :-

→ The function of the subtractor is to provide an output which is equal to the difference of two input signals.



→ Here, one signal is applied at the inverting terminal while the second signal is applied at the non-inverting terminals of an OP-AMP.

→ By Applying Superposition theorem, V_1 is active & V_2 is Grounded.



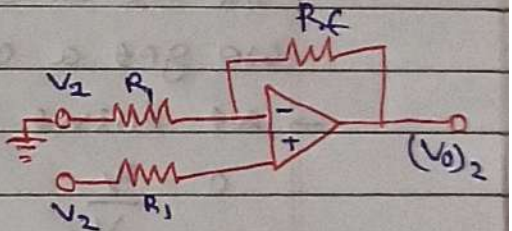
$$A_V = -\frac{R_f}{R_1} \Rightarrow \frac{(V_o)_1}{V_i} = -\frac{R_f}{R_1}$$

(closed loop inverting ckt)

Here V_1 is active, so the input voltage $V_i = V_1$

$$\Rightarrow \boxed{(V_o)_1 = -\left(\frac{R_f}{R_1}\right)V_1} \quad -(1)$$

→ By Applying Superposition theorem, V_2 is active & V_1 is Grounded.



$$A_V = \left(1 + \frac{R_f}{R_1}\right) \quad \text{(Non-inverting ckt)} \qquad \text{(closed loop non-inverting ckt)}$$

$$\Rightarrow \frac{(V_o)_2}{V_i} = 1 + \frac{R_f}{R_1}$$

$$\Rightarrow \frac{(V_o)_2}{V_2} = \frac{R_f}{R_1} \quad (\because V_i = V_2, \frac{R_f}{R_1} >> 1)$$

$$\Rightarrow \boxed{(V_o)_2 = \left(\frac{R_f}{R_1}\right)V_2} \quad -(2)$$

* Total output $V_o = (V_o)_1 + (V_o)_2$

$$= -\left(\frac{R_f}{R_1}\right)V_1 + \frac{R_f}{R_1}(V_2)$$

$\Rightarrow V_0 = \frac{R_f}{R_1}(V_2 - V_1)$

$\Rightarrow \boxed{V_0 = K(V_2 - V_1)}$ — (3) $(\because K = R_f/R_1)$

* Eqn (3) shows that output voltage is proportional to the difference of two input voltages.

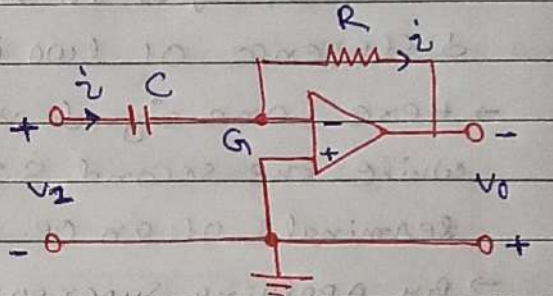
Case-(1) If $R_f = R_1$

then $\boxed{V_0 = V_2 - V_1}$ — (4)

Thus, the output voltage is equal to the difference of two input voltages.

Differentiator :-

→ The function of the differentiator is to give an output voltage which is proportional to the rate of change of the input voltage.



→ The circuit of a differentiator is the same as that of an inverting OP-AMP except that the input resistance (R_1) is replaced by a capacitor.

→ If we linearly increasing voltage to the differentiator, we get a constant d.c output.

→ At point 'G', the value of capacitor

$C = \frac{q}{V_1} \Rightarrow \boxed{V_1 = \frac{q}{C}}$ — (1) (where q = charge on capacitor)

Derivative both side of Eqn (1)

$\Rightarrow \frac{d}{dt}(V_1) = \frac{1}{C}\frac{dq}{dt}$

$\Rightarrow \boxed{\frac{d}{dt}(V_1) = \frac{i}{C}}$ $(\because \frac{dq}{dt} = i)$ — (2)

$\Rightarrow \boxed{i = C\frac{d}{dt}(V_1)}$

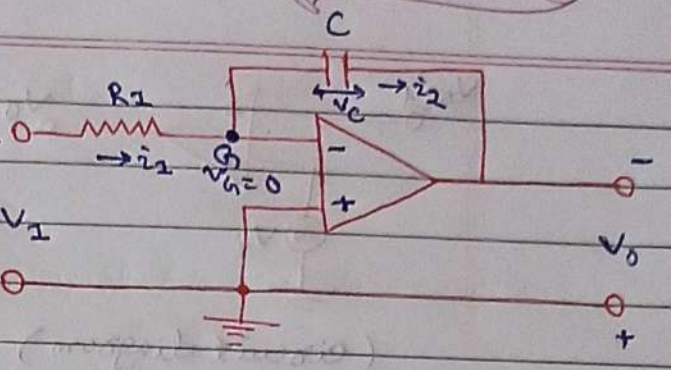
Again $\boxed{V_0 = -iR}$ — (3)

Substitute the value of Eqn (2) in Eqn (3)

$V_0 = -C\frac{d}{dt}(V_1) \cdot R \Rightarrow \boxed{V_0 = -CR\frac{dV_1}{dt}}$ — (4)

* Output voltage (V_0) is equal to a constant (CR) of derivative of the input voltage (V_1).

Integrator -:



→ The OP-amp integrator is an electronic integration circuit.

→ It performs the mathematical operation of integration with respect to time. (i.e. its output voltage is proportional to the input voltage integrated over time).

→ The integrator is an inverting OP-AMP in which feed-back resistor(R_f) has been replaced by a capacitor(C)

Mathematical derivation -:

Applying KCL on point 'G'.

$$i_1 - i_2 = 0 \Rightarrow i_1 = i_2 \qquad \left(\because i_1 = \frac{V_1}{R_1}\right)$$

As we know $C = \frac{q}{V_C} \Rightarrow q = CV_C \qquad \left(\because i_2 = C\frac{dV_C}{dt}\right)$

$$\Rightarrow \frac{dq}{dt} = C\frac{dV_C}{dt}$$

then $i_1 = i_2$

$$\Rightarrow \frac{V_1}{R_1} = C\frac{dV_C}{dt} \qquad \left(V_C = V_G - V_0 = 0 - V_0 = -V_0\right)$$

$$\Rightarrow \frac{V_1}{R_1} = -C\frac{d}{dt}(V_0)$$

$$\Rightarrow d(V_0) = -\frac{V_1}{R_1 C}\,dt$$

Integrate both side (LHS & RHS)

$$\Rightarrow \boxed{V_0 = -\frac{1}{R_1 C}\int V_1 \cdot dt}$$

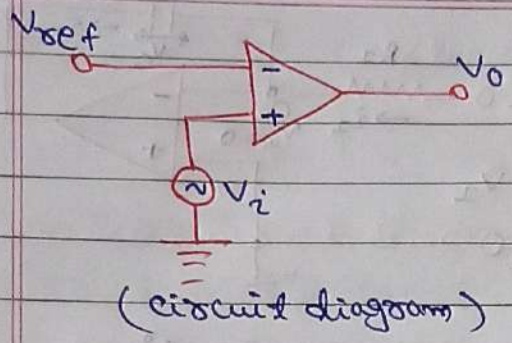
Comparator -:

→ comparator is a circuit which compares two voltages and provides an output that indicates the relation-ship between them.

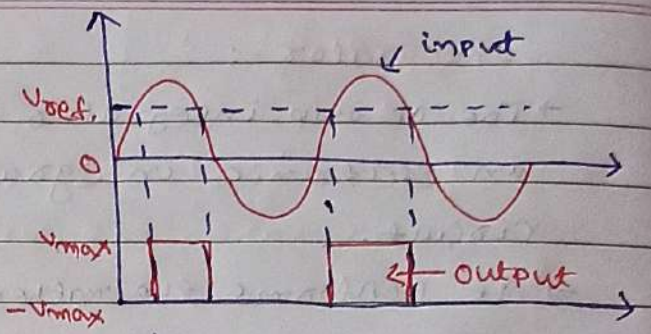
→ Comparator may be used to compare -:

⇒ Two changing voltages like two sine waves.

⇒ A changing voltage with a set d.C. reference voltage.



(circuit diagram)



(Input-output waveform)

→ Here, the OP-AMP is operated in open-loop configuration.

→ The input voltage is applied to the non-inverting input terminal and a set D.C. reference voltage (V_{ref}) is applied to the inverting terminal of the OP-AMP.

→ The output voltage (V_o) is varying from V_{max} to $-V_{max}$ or vice versa.